INVESTIGATION INTO THE USE OF A FOUR-CHANNEL SEQUENCY DIVISION MULTIPLEXING SYSTEM FOR THE TRANSMISSION OF DIGITAL DATA.

by

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DECLARATION

I, Hendrik Frank Coetzer, hereby declare that this dissertation which has been submitted to Technikon Free State for the award of the degree MAGISTER TECHNOLOGAIE: Engineering: Electrical, is my own unaided work and has not previously been submitted by me or any other person for the award of a qualification

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1999-03-18

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Student

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SYNOPSIS

Data communications in applications such as telecommunications, telemetry and data networks has become an integral part of everyday life and considerable research is conducted into methods of increasing signalling speed and reliability of data communications systems, while reducing costs at the same time.

At present many multi-channel systems employ frequency division multiplexing (FDM) and time division multiplexing (TDM) techniques to combine the input signals of several channels onto a common communications link. In this regard the use of sequency division multiplexing (SDM) offers a number of advantages over the more conventional methods of multiplexing.

Orthogonal rectangular waveforms are employed as carriers for the modulator and demodulator circuits in a SDM system. The set of Walsh functions; *Wal*(1,*t*), *Wal*(2,*t*), *Wal*(3,*t*), *Wal*(4,*t*) were used for this purpose. The unit pulse method employing block pulse waveforms was used to generate the set of Walsh functions.

Two different techniques of sequency division multiplexing were investigated in this project, viz; multi-level and binary systems of SDM. During the course of the project an adaptive method of slicing the multi-level modulator output signals was developed to produce binary SDM signals that switch between logic 1 and logic 0.

The multi-level and binary systems both provided for four channels, each operating at a signalling speed of 1 200 bits per second. Data input signals to each channel modulate a Walsh carrier and the modulator outputs are combined to produce a multi-level signal. In binary systems of SDM this multi-level signal must be converted to a binary signal that switches between logic 1 and logic 0.

Both systems of SDM have an inherent delay of 1 data bit.

All the necessary circuits were designed and built to permit testing of both systems of SDM.

Performance tests were conducted on both systems to determine the bit error rate for each channel for different values of signal to noise ratio. These tests were repeated using low pass filters with cut-off frequencies of 22,5kHz, 27kHz and 58,9kHz in the line simulator.

The results show that sequency multiplexing of digital data is a viable alternative to other methods of multiplexing. However, as SDM requires a larger bandwidth than conventional methods it's applications would be better suited to communications links such as co-axial cable or single wire links such as in telemetry systems for the control of irrigation equipment.

UITTREKSEL

Datakommunikasie in toepassings soos telekommunikasie, telemetrie en data netwerke het 'n noodsaaklike kenmerk van die moderne lewe geword en aansienlike navorsing het gelei tot metodes wat die oorseinspoed vermeerder en die akkuraatheid verbeter terwyl kostes beperk word.

Baie multi-kanaal sisteme maak tans van frekwensiedeelmultipleksering (FDM) en tyddeelmultipleksering (TDM) tegnieke gebruik om die insetseine van 'n aantal kanale te kombineer vir oorseining op 'n gemeenskaplike kommunikasie skakel. Die gebruik van sekwensiedeelmultipleksering (SDM) bied in hierdie geval 'n aantal voordele bo die meer konvensionele metodes van multipleksering.

Ortogonale reghoekige golfvorms word as draaggolwe vir die modulator en demodulator kringe in 'n SDM sisteem gebruik. Die stel Walsh funksies *Wal*(1,*t*), *Wal*(2,*t*), *Wal*(3,*t*), *Wal*(4,*t*) word vir hierdie doel aangewend. Die enkelpuls metode met blokpulsgolfvorms is gebruik om die stel Walsh funksies op te wek.

Twee verskillende metodes van sekwensiedeelmultipleksering is ondersoek, nl; multi-vlak en binêre sekwensiemultipleksering. Gedurende die verloop van die projek is 'n aanpasbare metode van sny van die multi-vlak modulator uitsetseine ontwikkel om binêre SDM seine vanuit die multi-vlak uitsette van die modulators te produseer. Die binêre seine skakel tussen die logika 1 en logika 0 vlakke.

Die multi-vlak en binêre sisteme maak voorsiening vir vier kanale. Elke kanaal werk teen 'n oorsein spoed van 1 200 bisse per sekonde. Data insetseine na elke kanaal moduleer 'n Walsh draaggolf en die modulator uitsette word gekombineer om 'n multi-vlak sein te produseer. In 'n binêre stelsel word die multi-vlak sein so gesny dat dit 'n binêre sein lewer wat tussen die logika 1 en logika 0 vlakke skakel. Daar is 'n inherente vertraging van 1 bis in beide SDM stelsels.

Al die nodige kringe is ontwerp, opgebou en saamgestel om die twee stelsels van SDM daar te stel vir die nodige toetse.

Werkverrigtingtoetse is uitgevoer om inligting te bekom i.v.m. die bisfouttempo ten opsigte van verskillende vlakke van ruis.

Werkverrigtingtoetse is op beide sisteme uitgevoer om die bisfoutempo te bepaal vir elke kanaal vir verskillende waardes van seinruisverhouding. Hierdie toetse is herhaal deur gebruik te maak van onderdeurlaatfilters met afsnyfrekwensies van 22,5kHz, 27kHz en 58,9kHz in die lynsimulator.

Die resultate toon dat sekwensiemultipleksering van digitale data 'n moontlike alternatief tot ander metodes van multipleksering is. Alhoewel, as gevolg daarvan dat SDM 'n groter bandwydte vereis as die konvensionele metodes, behoort dit beter geskik vir kommunikasie skakels te wees soos ko-aksiale kabel of enkeldraad skakels soos in telemetrie sisteme vir afstandsbeheer van besproeiingtoerusting.

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ABBREVIATIONS AND ACRONYMS USED

BPF	Band pass filter
Bit	Binary digit
Cal	Cosine Walsh
Ch	Channel
CPG	Clock pulse generator
DSM	Digital sequency multiplexing
FDM	Frequency division multiplexing
Hz	Hertz
kHz	Kilo-Hertz
kΩ	Kilo-ohm
LPF	Low pass filter
LSB	Least significant bit
MHz	Mega-Hertz
MSB	Most significant bit
MΩ	Meg-ohm
μF	Micro-Farad
nF	Nano-Farad
Osc	Oscillator
Ω	Ohm
pF	Pico-Farad
Rad	Rademacher
SDM	Sequency division multiplexing
Sal	Sine Walsh
Sign	Signum
SSB	Single sideband
TDM	Time division multiplexing
Wal	Walsh
WFG	Walsh function generator
zps	Zero crossings per second

Chapter 1

1. INTRODUCTION

The essential requirements of communications systems may be summarised as speed and reliability. This is clearly illustrated by the fact that modern telecommunications, telemetry and data networks extend around the globe and penetrate the depths of space. Signals are transmitted over vast distances and suffer severe attenuation and mutilation by noise. As a result telecommunication engineers and technologists are continually searching for ways to improve the quality and reliability of equipment at acceptable cost.

At present many multi-channel data transmission systems employ either frequency division multiplexing (FDM) or time division multiplexing (TDM) techniques to accommodate a number of channels within the baseband of the communication link [2, pp. 180-183].

Sequency division multiplexing [SDM] offers a third alternative with reduced complexity of equipment and attendant savings in the use of filter and setting up adjustments [2, pp. 185-186].

1.1 OBJECTIVES OF THE RESEARCH AND EXECUTION OF THE PROJECT

The main objective of the research project was to design, construct and evaluate a four-channel system of sequency division multiplexing using a set of Walsh function carriers for the transmission of digital data at a rate of 1200 bits per second in each channel.

Two systems of SDM were constructed using multi-level and binary methods of SDM. A novel slicer was developed for the binary SDM system to produce binary signals from the multi-level modulator outputs. A 16R4 programmable array logic (PAL) integrated circuit [19, pp. 24-119] was used to set the slicing level according to the various combinations of input data to the system.

As it was not necessary to develop carrier recovery techniques for this project the same Walsh function generator was used to provide carriers both for the multiplexer and demultiplexer circuits.

Input data for evaluation of the system was generated synchronously with the set of Walsh function carriers.

All the necessary circuits for these systems were built on veroboard using the 74 series of digital integrated circuits with FET input LF353 and TL081 operational amplifiers for the linear parts of the circuitry.

Test equipment such as a random number generator, line simulator with a white noise generator and low pass filters, bit error detector and binary counters were designed and built to evaluate system performance. Two 16R8 PAL integrated circuits [19, p. 24-117] were used to construct the pseudo random number generator.

Bit error rate measurements on the multi-level and binary SDM systems revealed that the cut-off frequency of the low-pass filter in the line simulator has a profound effect upon the bit error rate (BER) of both systems.

The research procedure of this project is outlined by the flowchart in Fig. 1.1.

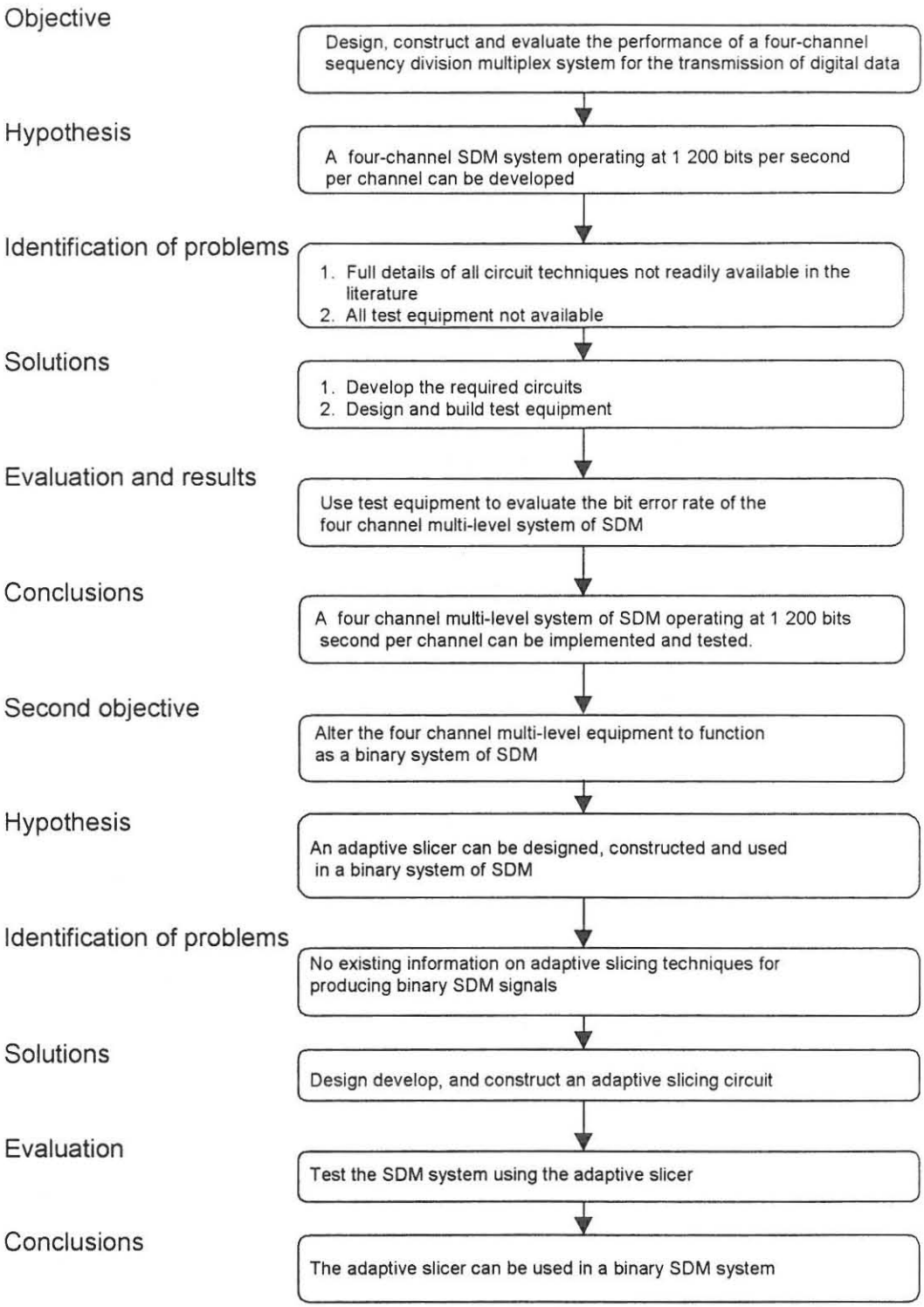


Fig. 1.1 *Research phases of the project*

1.2 STRUCTURE OF THE DISSERTATION

The flowchart in Fig. 1.2 shows the structure of the dissertation.

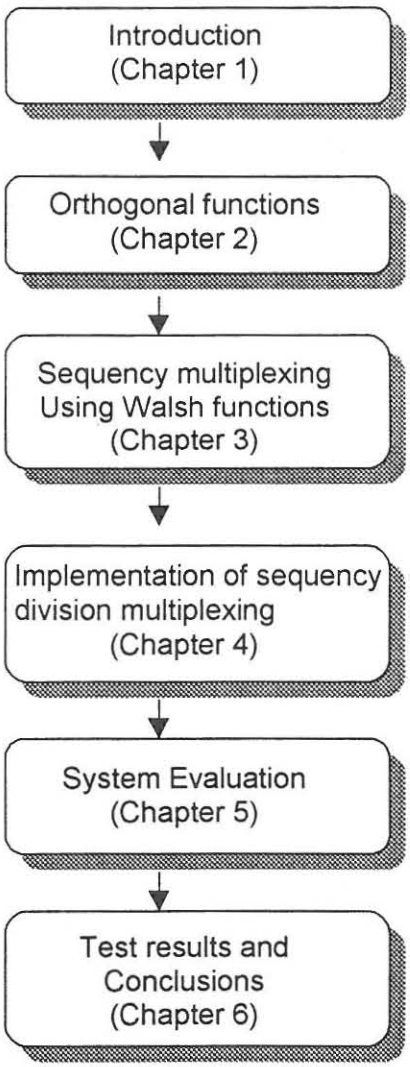


Fig. 1.2 *Structure of the dissertation*

Fundamental aspects of orthogonal functions, with particular reference to the Walsh functions, are introduced followed by the basic principles of sequency division multiplexing.

Implementation of the multi-level and binary systems of SDM is described, firstly on a block diagram basis with waveforms to illustrate the action of the system and then the various circuits and techniques used are discussed.

Details are given of the test and evaluation equipment as well as the procedures followed in evaluation of the system.

Results obtained are given with conclusions regarding the BER of the two systems in the presence of noise for different cut-off frequencies of the low-pass filter in the line simulator.

Chapter 2

ORTHOGONAL FUNCTIONS

2.1 INTRODUCTION

The work in this project is mainly concerned with the use of orthogonal square waveforms as carriers in a multi-channel system for the transmission of digital information. The set of square waveforms used as carriers are known as "Walsh functions".

This presentation of the theoretical background commences with an explanation of the terms "orthogonal", "complete" and "sequency". This is followed by a brief introduction to certain relevant square wave functions leading up to the Walsh functions and the way in which they may be derived from Rademacher or block pulse functions.

2.2 ORTHOGONALITY

The principle of orthogonality will first be introduced with reference to vectors, and then extended to include time related functions. The analogy between vectors and signals is more than co-incidental. The use of the more familiar geometric ideas often prove very useful in gaining added perspective into the handling of signal waveforms [23, p. 14].

If the angle between two vectors is a right angle they are said to be orthogonal or perpendicular to one another [18, p. 32].

Consider a three dimensional space with a set of rectangular co-ordinates X, Y, and Z at right angles to one another as in Fig. 2.1. The unit vectors a_1, a_2 and a_3 lie along the axes.

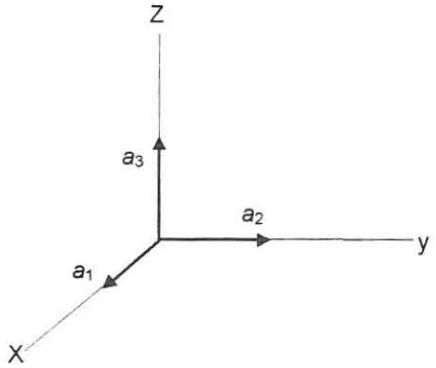


Fig. 2.1 *Rectangular co-ordinates with unit vectors a_1, a_2 and a_3.*

Let *F* be a vector in this three dimensional space with initial point 0 at the origin, and components $F_1.a_1$, $F_2.a_2$ and $F_3.a_3$ in the directions of the axes *x*, *y*, and *z* as in Fig. 2.2.

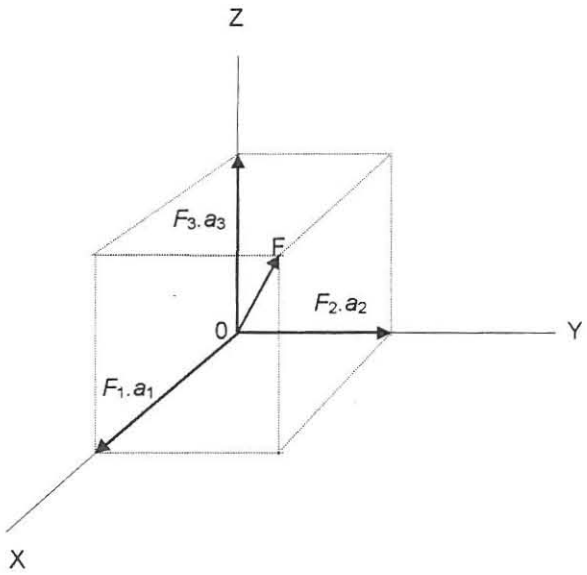


Fig. 2.2 *Vector F in three dimensional space*

From Fig. 2.2 it can be seen that [20, p. 22]:

$$F = \sum_i F_i.a_i \tag{2.1}$$

Where;

$$i = 1,2,3$$

Since any vector in this three dimensional space can be represented by a linear combination of the orthogonal unit vectors a_1, a_2, a_3, the system is said to be "complete". On the other hand, a vector in this space cannot be adequately represented by a linear combination of only two unit vectors such as a_1 and a_2. Such a two dimensional set is then said to be "incomplete" [20, p. 21].

These concepts can be extended to an *N* dimensional space if necessary.

The signals used in telecommunications work are usually time related. For example, a set of carrier waveforms may be written as;

$$f(t) = f_0, f_1, f_2..... \tag{2.2}$$

These functions will be orthogonal over the interval (0,*T*) when;

$$\int_0^T f_m(t).f_n(t).dt = 0 \qquad \text{if} \quad m \neq n \tag{2.3}$$

and

$$\int_0^T f_m(t).f_n(t).dt \neq 0 \qquad \text{if} \quad m = n \tag{2.4}$$

If the result is unity, the set is said to be "orthonormal" [3, p. 27].

When testing a particular function for orthogonality, it must be compared with another function having the same variable. For example, although the functions *sin(a.t)* and *sin(b.t)* may be orthogonal, *sin(a.t)* and *sin(b.x)* are not, because *sin(a.t)* is a function of time, t, and *sin(b.x)* is a function of some other variable, *x* [15, p. 283].

The circular functions, *sine* and *cosine*, are the most well known and frequently used orthogonal functions in the field of communications engineering. The orthogonality of these functions over an interval ($0 < t < T$) may be tested as follows;

Let

$$f_m(t) = \sqrt{2}.\cos(2.\pi.m.t) \qquad \text{and} \qquad f_n(t) = \sqrt{2}.\cos(2.\pi.n.t)$$

then

$$\int \sqrt{2}.\cos(2.\pi.m.t).\sqrt{2}.\cos(2.\pi.n.t)dt$$

$$= \int \cos[2.\pi.(m+n).t]dt + \int \cos[2.\pi.(m-n).t]dt \qquad (2.5)$$

However, the area under a sinusoidal or co-sinusoidal waveform for a complete period $T = 1/f$ is zero. Therefore, if $m \neq n$ and both m and n are integers, the result of the above calculation will be zero.

When $m = n$,

$$\int \sqrt{2}.\cos(2.\pi.m.t).\sqrt{2}.\cos(2.\pi.n.t)dt$$

$$= \int 2.\cos^2(2.\pi.m.t)dt$$

and the result will have a finite value [2, p. 5].

Since the functions $f_m(t)$ and $f_n(t)$ satisfy the above conditions when $m = n$ and $m \neq n$, they are said to be orthogonal.

2.3 SEQUENCY

The zero crossings of sinusoidal functions (periodic functions) are uniformly spaced over an interval of time and the term "frequency" is used to denote the number of complete cycles (or, one half the number of zero crossings) generated by the sinusoidal functions per unit time.

Certain functions, however, do not have a regular period and the zero crossings occur at differing time intervals. The term "frequency" is, therefore, not applicable to these aperiodic functions.

This is illustrated by the waveforms of $f_1(t)$, $f_2(t)$, and $f_3(t)$ in Fig. 2.3.

The sinusoidal function $f_1(t)$ in Fig. 2.3 is periodic and has four zero crossings in the given interval. The square wave, $f_2(t)$, is also periodic with four zero crossings. However, although the function, $f_3(t)$, also has four zero crossings, its period is irregular and it is said to be "aperiodic."

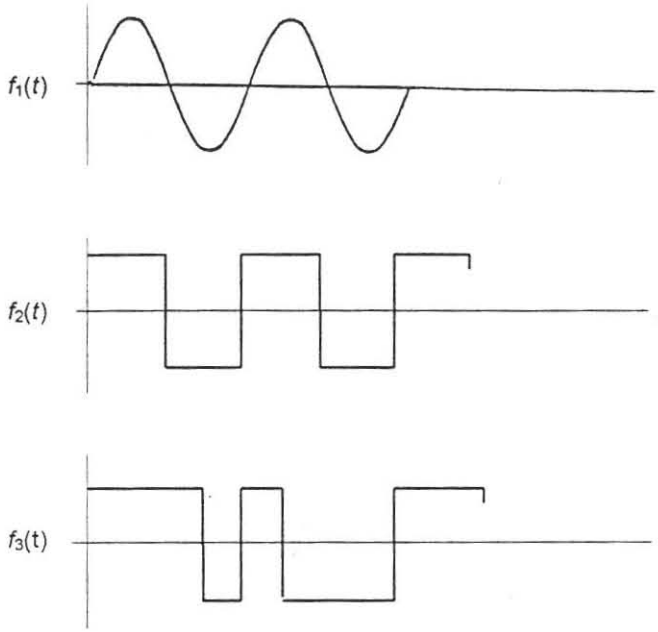


Fig. 2.3 *Waveforms of periodic and aperiodic functions.*

The waveforms $f_1(t)$ and $f_2(t)$ are signals with a fixed period, while the period of the waveform $f_3(t)$ fluctuates.

A generalisation of frequency may be effected by defining it as "one half the average number of zero crossings per unit time", and the term "sequency" is used in place of "frequency". Sequency may be applied to either the periodic, or aperiodic functions.

While frequency is expressed in hertz, the notation zps (zero crossings per second) is used for the sequency of a waveform. This also corresponds with half the number of sign changes per second [26, pp. 8-9].

2.4 RADEMACHER FUNCTIONS

The Rademacher functions consist of a series of square waves with unit mark-space ratio. Waveforms of the first six Rademacher functions are given in Fig. 2.4.

The magnitude of the first function, $Rad(0,t)$, is equal to one over the entire interval $0 < t < T$.

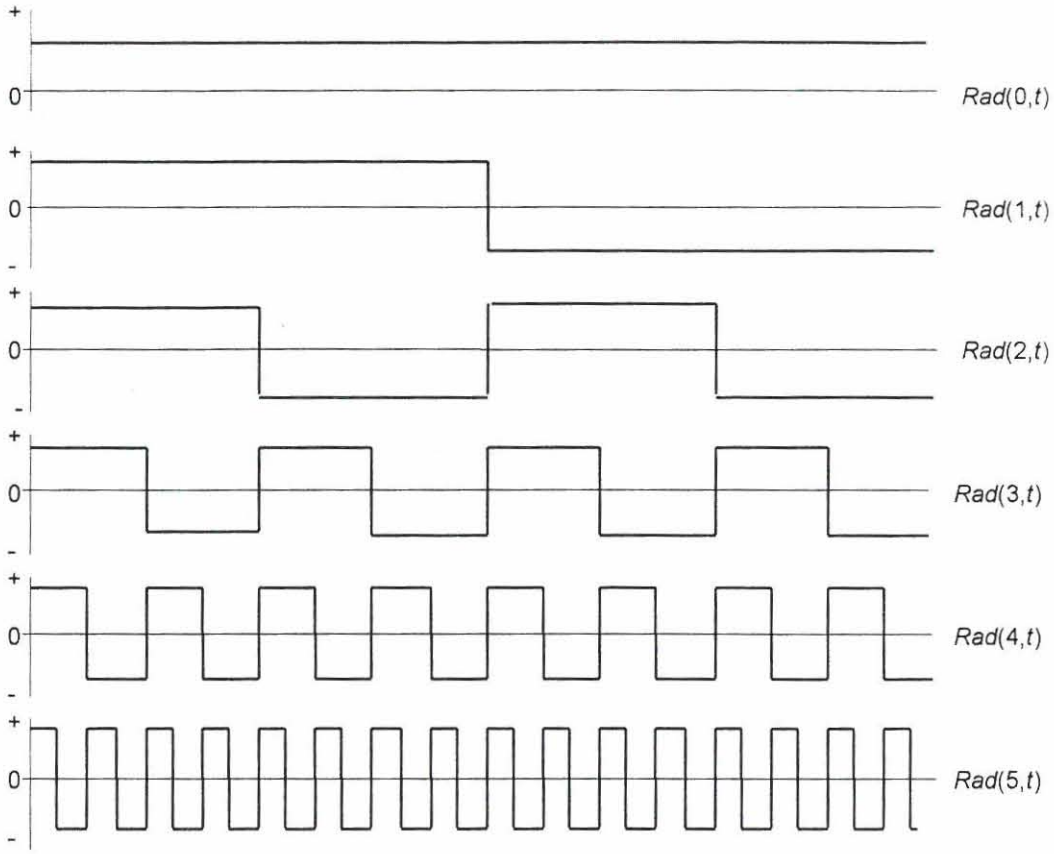


Fig. 2.4 *A set of six Rademacher functions*

The set of Rademacher functions may be derived from sinusoidal functions with the aid of the formula [2, p. 9]:

$$Rad\ (n,t) = Sign[sin(2^n.\pi.t)] \qquad (2.6)$$

The function, *Sign (Signum),* represents an ideal limiter which turns a sine wave into a square wave that switches between +1 and -1.

The Rademacher functions are important principally because other series, such as the Walsh functions, can be derived from them [2, p. 9].

2.5 WALSH FUNCTIONS

The Walsh functions are a set of rectangular waveforms with amplitude +1 and -1 [9, p. 694]. Unlike the Rademacher functions, the Walsh functions do not have a unit mark-space ratio. A set of eight Walsh functions are shown in Fig. 2.5.

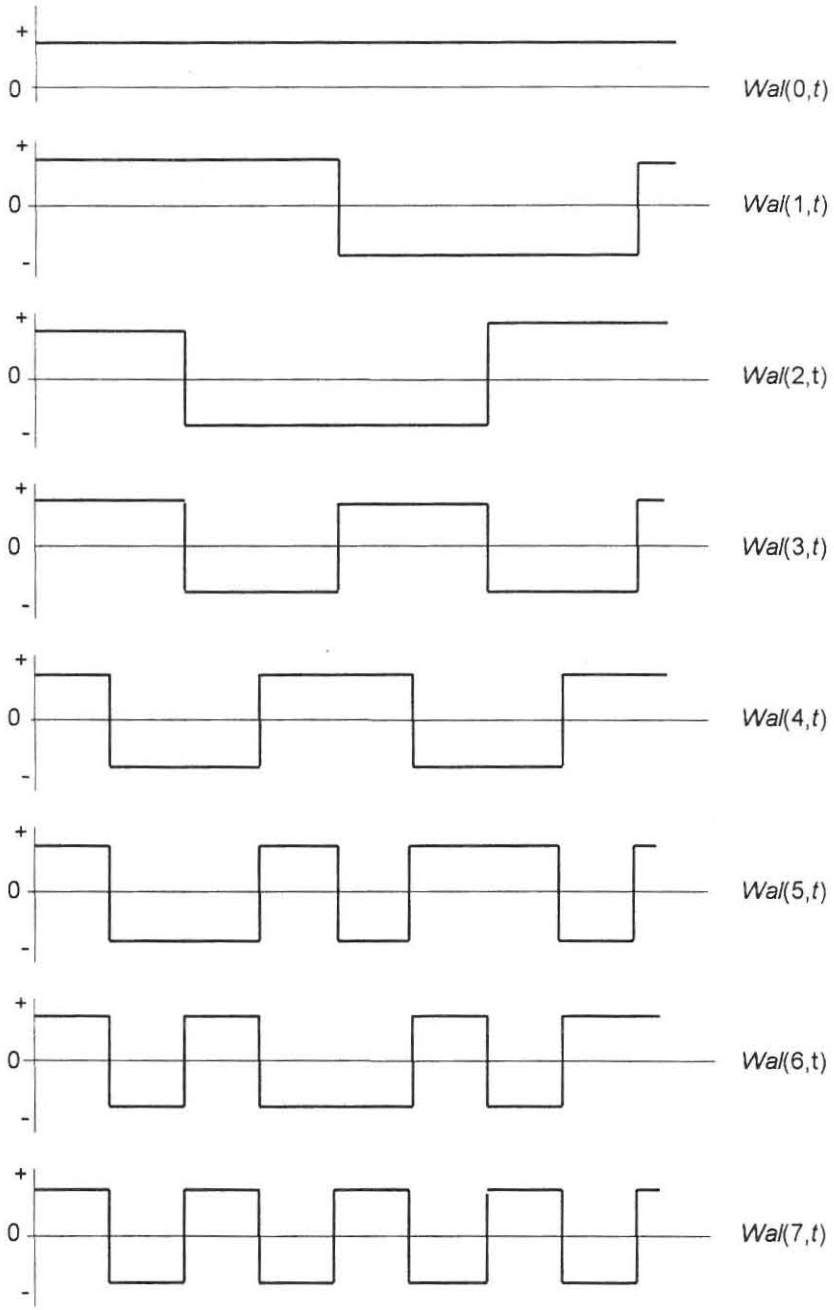


Fig. 2.5 *A set of eight Walsh functions*

2.5.1 ORTHOGONALITY OF WALSH FUNCTIONS

Walsh functions have the property that the product of two Walsh functions yields another Walsh function [26, p. 241].

$$Wal(h,t) \cdot Wal(k,t) = Wal(h \oplus k,t) \tag{2.7}$$

Here $(h \oplus k)$ denotes modulo 2 addition of h and k. Both h and k must be expressed in binary form. Except for $Wal(0,t)$ which has no period, every Walsh function has an integral number of cyclic periods in the unit interval $0 \leq t \leq 1$, and hence its integral (average height or area) over this interval is zero.

Then, it follows that every Walsh function is orthogonal to each of the other Walsh functions, as $(h \oplus k)$ can only be zero when $h = k$. Furthermore, when $h = k$, the process of integration yields a solution of 1 and the series is said to be "orthonormal" [26, p. 258].[1]

2.6 DERIVATION OF WALSH FUNCTIONS

The Walsh function series can be obtained in a number of ways. Four methods of generating Walsh functions are outlined below.

2.6.1 RECURSIVE RELATIONS

A set of Walsh functions of order k can be defined over an interval $0 \leq t \leq 1$ as follows;

Let 2^m be any power of 2 that equals or exceeds k. For example, if the first eight Walsh functions are to be described, use $m = 3$.

The integer k can be expressed in the form;

$$k = \sum_r 2^r . k_r \tag{2.8}$$

[1] See parag.2.2.

$r = 0.....(m-1)$

Where k_r is the binary value of k, eg; 000,001,010.....

Then, for all values of t [26, p. 258]:

$$Wal(k,t) = \prod_r Sign\left[\cos^{k_r}\left(2^r.\pi.t\right)\right] \tag{2.9}$$

Values of k, k_r and m are set out in Table 2.1 for $Wal(0,t)$ to $Wal(7,t)$.

Table 2.1 Tabulation of variables for $Wal(k,t)$.

k	k_r	m
0	000	3
1	001	3
2	010	3
3	011	3
4	100	3
5	101	3
6	110	3
7	111	3

The Walsh functions can now be evaluated using equation (2.9).

For example;

$$Wal(5,t) = \prod_r Sign\left[\cos^{101}\left(2^r.\pi.t\right)\right]$$

Here

$$k = 5, \quad k_r = (101)_2 \text{ and } r = 0.....2$$

Then;

$$Wal(5,t) = Sign[\cos^1(2^0.\pi.t)].Sign[\cos^0(2^1.\pi.t)].Sign[\cos^1(2^2.\pi.t)]$$

Simplifying;

$$Wal(5,t) = Sign[\cos(\pi.t)].Sign[\cos(4.\pi.t)]$$

The waveforms of *Sign*[*cos*($\pi.t$)] and *Sign*[*cos*(4.$\pi.t$)] are plotted separately in Fig. 2.6(a) and (b) and their product, representing *Wal*(5,*t*), in Fig. 2.6(c).

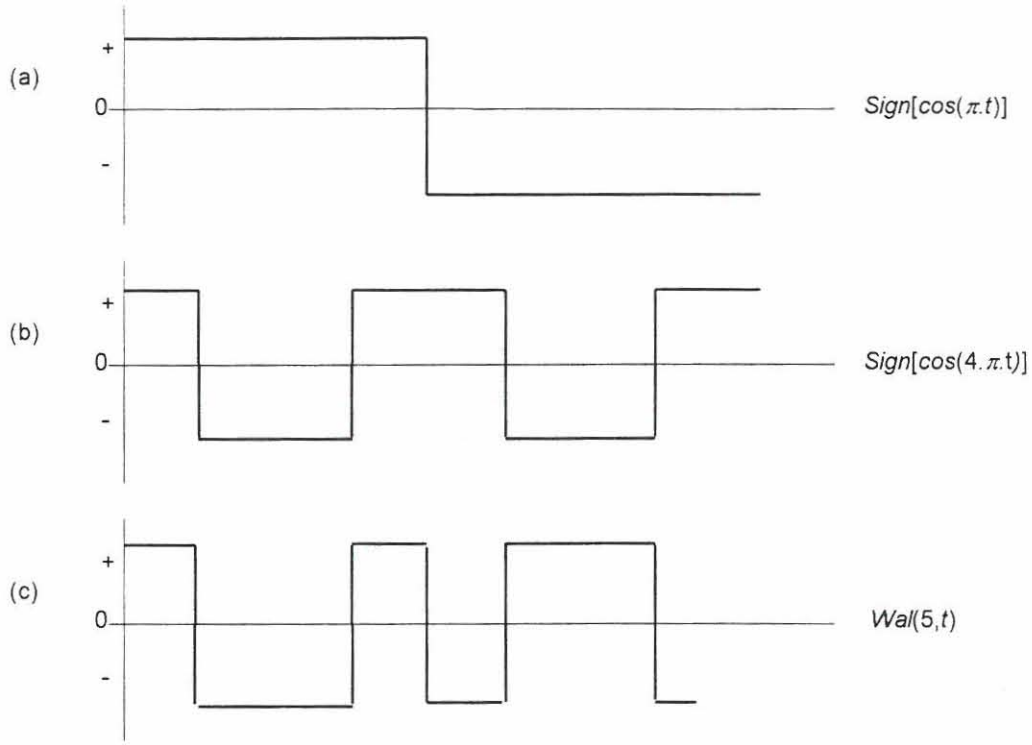


Fig. 2.6 *Derivation of Wal*(5,*t*) *from Sign*[*cos*($\pi.t$)] *and Sign*[*cos*(4.$\pi.t$)]

2.6.2 PRODUCTS OF RADEMACHER FUNCTIONS

The Walsh functions may be written in terms of the Rademacher functions as follows [15, p. 285]:

$$Rad(k, t) = Wal[2^k - 1, t] \qquad (2.10)$$

$$k = 0,1,2.....$$

Then,

$$Wal(0,t) = Rad(0,t)$$

$$Wal(1,t) = Rad(1,t)$$

$$Wal(3,t) = Rad(2,t)$$

$$Wal(7,t) = Rad(3,t) \quad \text{etc.}$$

The remaining Walsh functions may be derived by making use of the property that the product of two Walsh functions yields another Walsh function such that;

$$Wal(i,t).Wal(j,t) = Wal(i \oplus j,t), \text{ where } (i \oplus j) \text{ denotes modulo 2 addition.}^{2}$$

An example will illustrate the use of this relationship.

Suppose that it is necessary to find an expression for $Wal(2,t)$ in terms of the Rademacher functions. Writing $Wal(2,t)$ in binary notation;

$$Wal(2,t) = Wal(010_2,t)$$

Now it is necessary to find two binary numbers whose modulo-2 sum is equal to 010_2, such as;

$$001_2 \oplus 011_2 = 010_2$$

ie. $Wal(1 \oplus 3,t) = Wal(2,t)$

$$\therefore \quad Wal(2,t) = Wal(1,t).Wal(3,t)$$

$$= Rad(1,t).Rad(2,t)$$

This result may be verified by referring to the waveforms in Fig. 2.7.

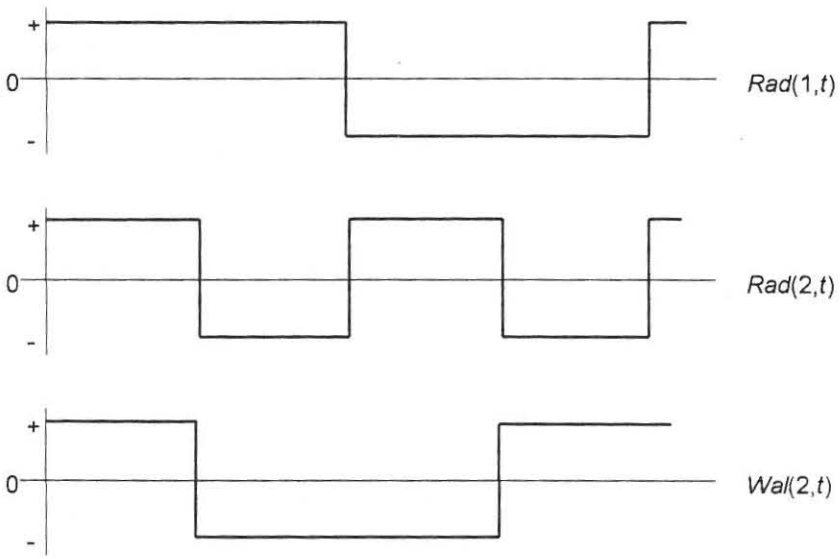


Fig. 2.7 *Derivation of Wal(2,t) from Rad(1,t) and Rad(2,t)*

[2] see expression 2.7.

If the magnitudes of *Rad*(1,*t*) and *Rad*(2,*t*) are multiplied, instant by instant, the waveform of *Wal*(2,*t*) will result.

Similarly,

$$Wal(4,t) = Rad(2,t).Rad(3,t)$$

2.6.3 HADAMARD MATRIX

The Hadamard matrix, *H*, is a square array whose co-efficients comprise only +1 and -1 [2, p. 62]. The rows (and columns) of the matrix are orthogonal to one another. Rows and columns may be interchanged, and the signs of every element in a row or column may be changed without affecting the orthogonal properties of the matrix. The first two orders of the Hadamard matrix are;

$$H_1 = [1] \tag{2.11}$$

$$H_2 = \begin{bmatrix} 1 & 1 \\ 1 & -1 \end{bmatrix} \tag{2.12}$$

Higher order matrices can be obtained through Kronecker multiplication [2, p. 62].

The Kronecker product is obtained by replacing each element in the given matrix by the matrix H_2 in (2.12) above.

If *H* is a Hadamard matrix of order *N*, the matrix;

$$G = \begin{bmatrix} H & H \\ H & -H \end{bmatrix} \tag{2.13}$$

is a Hadamard matrix of order 2.*N* [26, p. 300].

In this way a Hadamard matrix of order 4 is obtained using the Kronecker product $H_2 \otimes H_2$, where the symbol $\otimes$ is used to denote Kronecker multiplication.

Then,

$$H_4 = \begin{bmatrix} H_2 & H_2 \\ H_2 & -H_2 \end{bmatrix} = \begin{bmatrix} 1 & 1 & 1 & 1 \\ 1 & -1 & 1 & -1 \\ 1 & 1 & -1 & -1 \\ 1 & -1 & -1 & 1 \end{bmatrix} = \begin{bmatrix} Had(0,t) \\ Had(1,t) \\ Had(2,t) \\ Had(3,t) \end{bmatrix} \quad (2.14)$$

And,

$$H_8 = \begin{bmatrix} 1 & 1 & 1 & 1 & 1 & 1 & 1 & 1 \\ 1 & -1 & 1 & -1 & 1 & -1 & 1 & -1 \\ 1 & 1 & -1 & -1 & 1 & 1 & -1 & -1 \\ 1 & -1 & -1 & 1 & 1 & -1 & -1 & 1 \\ 1 & 1 & 1 & 1 & -1 & -1 & -1 & -1 \\ 1 & -1 & 1 & -1 & -1 & 1 & -1 & 1 \\ 1 & 1 & -1 & -1 & -1 & -1 & 1 & 1 \\ 1 & -1 & -1 & 1 & -1 & 1 & 1 & -1 \end{bmatrix} = \begin{bmatrix} Had(0,t) \\ Had(1,t) \\ Had(2,t) \\ Had(3,t) \\ Had(4,t) \\ Had(5,t) \\ Had(6,t) \\ Had(7,t) \end{bmatrix} \quad (2.15)$$

If the rows of this matrix are rearranged in ascending order of sequency, a Walsh matrix results [2, p. 108].

$$W_8 = \begin{bmatrix} 1 & 1 & 1 & 1 & 1 & 1 & 1 & 1 \\ 1 & 1 & 1 & 1 & -1 & -1 & -1 & -1 \\ 1 & 1 & -1 & -1 & -1 & -1 & 1 & 1 \\ 1 & 1 & -1 & -1 & 1 & 1 & -1 & -1 \\ 1 & -1 & -1 & 1 & 1 & -1 & -1 & 1 \\ 1 & -1 & -1 & 1 & -1 & 1 & 1 & -1 \\ 1 & -1 & 1 & -1 & -1 & 1 & -1 & 1 \\ 1 & -1 & 1 & -1 & 1 & -1 & 1 & -1 \end{bmatrix} = \begin{bmatrix} Wal(0,t) \\ Wal(1,t) \\ Wal(2,t) \\ Wal(3,t) \\ Wal(4,t) \\ Wal(5,t) \\ Wal(6,t) \\ Wal(7,t) \end{bmatrix} \quad (2.16)$$

A frequency (sequency) interpretation of the matrix arises when one examines the number of sign changes in each row.

The rows of the matrix may be regarded as being equivalent to rectangular waveforms of amplitude ±1. These are the Walsh functions arranged in order of sequency (sequency or Walsh ordering) [26, p. 300].

The Walsh functions are special Hadamard functions and further systems of functions can be derived from them by permutations of the rows and columns, and

by sign inversion. Permutation of rows only leads to a different numbering of the waveforms in the sequence and has no effect on the behaviour of the system. However, by permutation of the columns, and inversion of column signs, it is possible to generate sets of carriers which could lead to different results in the transmission system [11, p. 181].

2.6.4 BLOCK PULSE FUNCTIONS

The block pulse functions are an orthogonal set of rectangular waveforms. The amplitude of only one of these waveforms may differ from 0 at any one time. A set of block pulse functions are illustrated in Fig. 2.8.

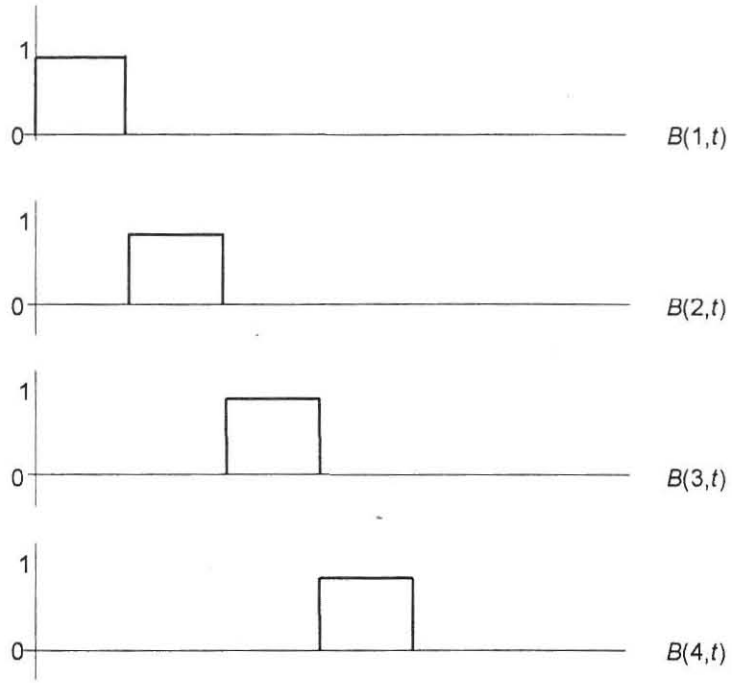


Fig. 2.8 *A set of four block pulse functions*

Block pulse functions of order m may be defined on an interval $t \in [0, T]$ as follows [26, p. 228]:

$$\phi_i = 1 \text{ for } t \in \left[(i-1).\frac{T}{m}, i.\frac{T}{m}\right] \tag{2.17}$$

$\phi_i = 0$ elsewhere.

Thus, when viewed in the time domain the block pulse functions in Fig. 2.8 have unit amplitude and width *T/m*. The period of each waveform is *T*, and the repetition rate is 1/*T*.

The Walsh functions can be derived from the block pulse functions with a set of logic gates. In this way a set of block pulse functions have been used to generate the Walsh functions required for this project.[3]

2.7 SAL AND CAL FUNCTIONS [13, pp. 81-82]

The Walsh functions can be classified in terms of even and odd functions using:

$$Wal(2.k,t) = Cal(k,t) \tag{2.18}$$

and

$$Wal(2.k\text{-}1,t) = Sal(k,t) \tag{2.19}$$

where

$$k = 1,2.....N/2$$

This defines two further series having close similarities with the sine and cosine functions [2, p. 15].

These even and odd functions are analogous to the sine and cosine functions and they are denoted by *Sal* (*sine Walsh*) and *Cal* (*cosine Walsh*) [26, p. 15]. A set of *Sal* and *Cal* functions are shown in Fig. 2.9

When the range is defined as $-1/2 < t < 1/2$ the functions are either directly symmetrical about 0 (*Cal*) or inversely symmetrical (*Sal*) [2, p. 16].

[3] See paragraph 4.1.6.1

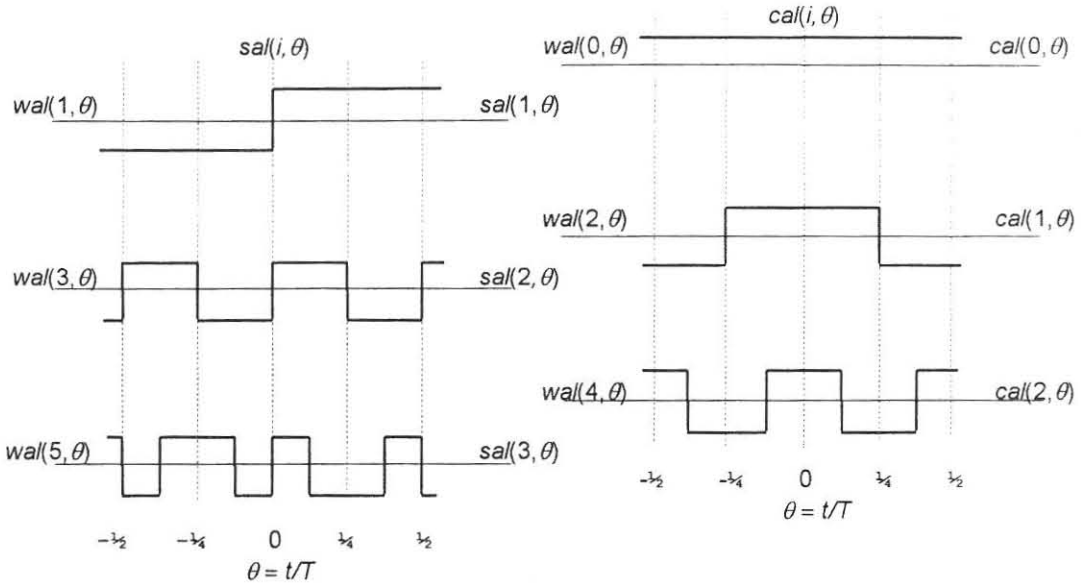


Fig 2.9 *A set of Sal and Cal functions*

2.8 Summary

- Functions $f_m(t)$ and $f_n(t)$ will be orthogonal over an interval $(0, T)$ when;

$$\int_0^T f_m(t).f_n(t).dt = 0 \qquad \text{if} \quad m \neq n$$

and

$$\int_0^T f_m(t).f_n(t).dt \neq 0 \qquad \text{if} \quad m = n$$

- A generalisation of frequency can be made by defining it as "one half the number of zero crossings of the waveform per unit time".

- Rademacher functions are a series of square wave functions which may be derived from sinusoidal functions using;

$$Rad\ (n,t) = Sign[sin(2^n.\pi.t)]$$

- Walsh functions are a complete set of orthogonal square waveforms which may be used to multiplex a number of channels of digital data.

- The Walsh functions may be derived in a number of ways. For example, using a set of recursive relations, products of Rademacher functions, or with the aid of the Hadamard matrix.

- Block pulse functions are also a set of rectangular waves and have been used to derive the Walsh functions in the equipment for this project. The amplitude of only one of the waveforms may differ from zero at any one time.

Chapter 3

SEQUENCY MULTIPLEXING USING WALSH FUNCTIONS

3.1 FREQUENCY DIVISION MULTIPLEXING (FDM)

Consider a number of baseband signals from *n* sources, each having a bandwidth of *B* Hz. These signals modulate *n* different carriers and are translated to another region in the frequency spectrum.

Amplitude modulation with single sideband (SSB) transmission is used in this example and the upper sideband of each modulator output is used for transmission purposes. After filtering, the outputs of the modulators are summed resulting in a signal with different frequency components [1, pp. 250-251]. The process is illustrated in Fig. 3.1.

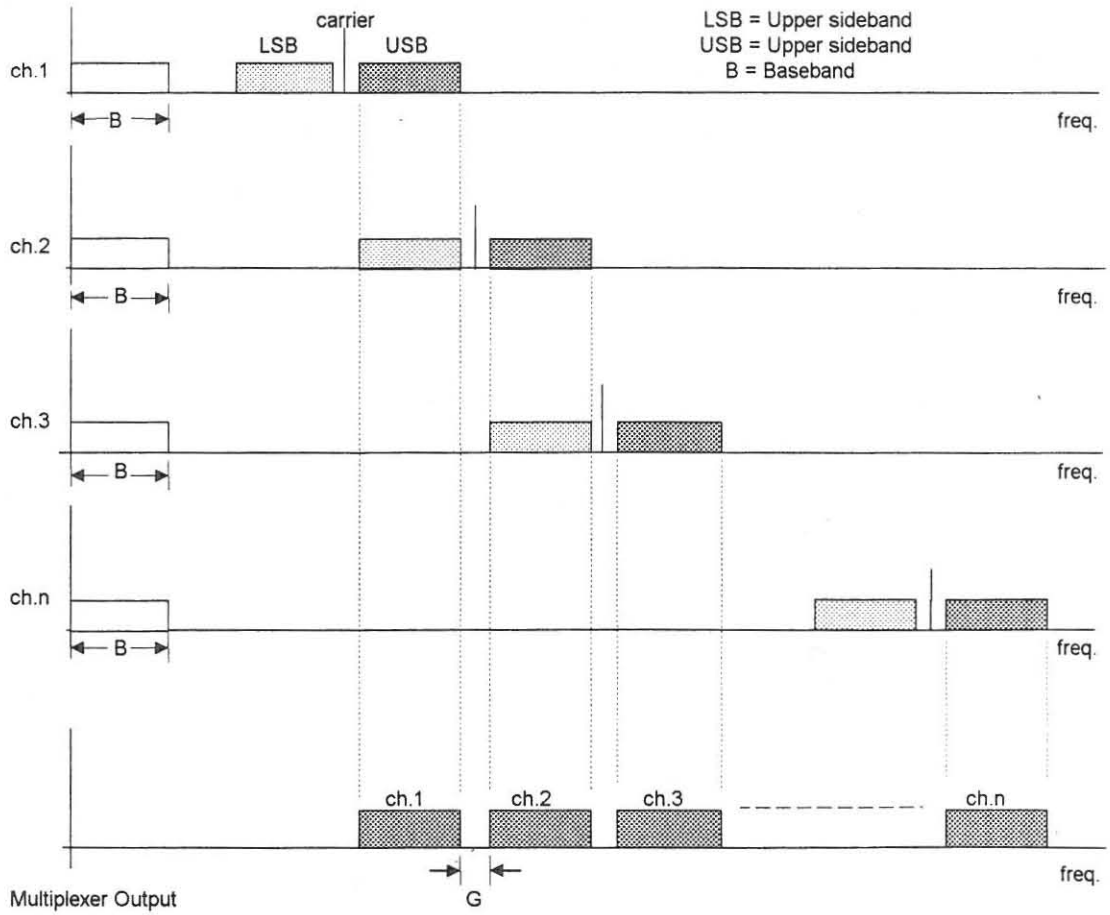


Fig. 3.1 *Principles of frequency division multiplexing*

A guard band, *G*, between channels ensures that the spectral range from one channel does not overlap with the spectral range of an adjacent channel. The total bandwidth required is then $\{n \cdot B + (n-1) \cdot G\}$ Hz. A basic block diagram arrangement of the frequency multiplexing technique is given in Fig. 3.2.

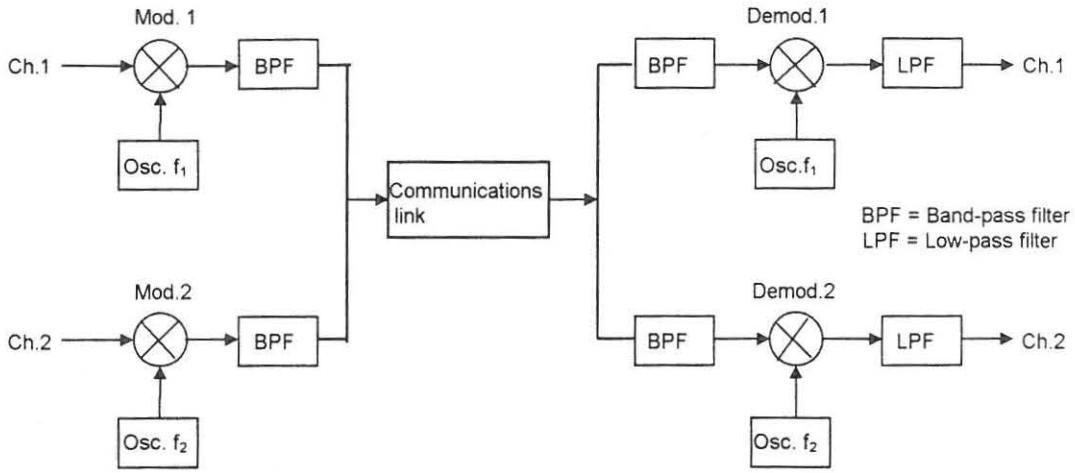


Fig 3.2 *Block diagram of basic two channel FDM system*

The input signal $S_i \cos\phi_i t$ in each channel, (Ch.), is effectively multiplied with its respective carrier $C_i \cos\omega_i t$ in the modulator, resulting in the production of upper and lower sidebands;

$$\frac{S_i \cdot C_i}{2} \cdot \left[\cos(\phi_i + \omega_i)t + \cos(\phi_i - \omega_i)t\right] \qquad (3.1)$$

These modulation products are band-pass filtered and summed to produce a composite signal. The filters ensure that only one sideband is passed through in each channel.

In this case (see Fig.3.1) the composite signal consists of the sum of all the upper sidebands, ie;

$$v(t) = \sum_i \frac{S_i \cdot C_i}{2} \cdot \cos(\phi_i + \omega_i)t \qquad (3.2)$$

$$i = 1,2.....n$$

This signal is transmitted over the communication link and a noise component, $N(t)$, will be combined with it resulting in a received signal:

$$E(t) = v(t) + N(t) \tag{3.3}$$

At the receiver, the channels are separated from one another with a number of band-pass filters. The signals are then demodulated by multiplying each with a replica of its carrier. The output from each demodulator will contain a component with the original signal [2, pp. 232-233]:

$$D(t) = A \cdot S_i \cos \phi_i t + Q \cdot N(t) \tag{3.4}$$

Where

A = Overall gain of the channel

Q = Fraction of total noise in the channel

3.2 TIME DIVISION MULTIPLEXING

With time division multiplexing (TDM) the set of input signals $S_i(t)$ are multiplexed in the time domain. These input signals must be sampled at a minimum rate of $2.f_m$, where f_m is the maximum frequency of the input signal. This is known as the "Nyquist rate" [24, p. 160]. The samples are transmitted over the communications link, one after another, as shown in Fig. 3.3.

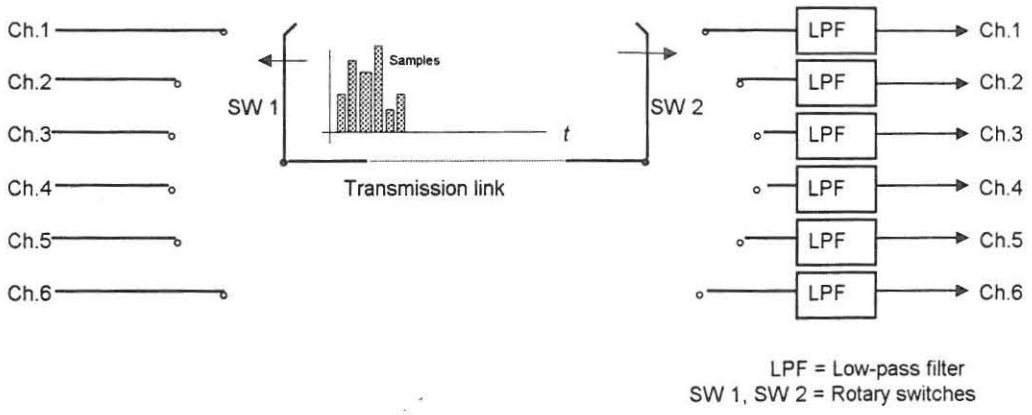


Fig. 3.3 *Basic principles of a six channel TDM system.*

As the sampling switch, SW 1, rotates, the samples S_1, S_2.....S_n from channels 1 to n are transmitted at a minimum rate of $2.n.f_m$ samples per second.

As shown in Fig. 3.3 the amplitude of the transmitted pulses is proportional to the signal amplitude at the time the sample is taken. This is known as pulse amplitude modulation (PAM).

At the receiver the samples are sorted into their respective channels with a rotating switch, SW 2. A low-pass filter in each channel recovers the original signals from among these samples [1, pp. 252-254].

3.3 SEQUENCY DIVISION MULTIPLEXING

3.3.1 BASIC PRINCIPLES.

Sequency division multiplexing (SDM) is similar to FDM in that the input signals also modulate carriers that are allocated to each channel. In other ways, as the Walsh functions are pulses, sequency division multiplexing resembles TDM. The input signals may be in analog form which are then sampled before multiplexing, or they may be data pulses in binary or other coded form [16, p. 659].

Each input signal modulates one particular Walsh function from the set of Walsh functions. The complete set of modulated Walsh functions is combined in a summation process and then transmitted.

At the receiver, the demodulator recovers the data in each channel by multiplying the composite waveform with locally generated replicas of the codewords used as Walsh function carriers. This is known as a pattern recognition system [8, p. 417].

An important advantage of SDM over FDM is that the modulation process produces only one sideband [22, p. 327], whereas FDM using amplitude modulation with sinusoidal carriers produces both upper and lower sidebands. Sideband filters are therefore not required in systems using SDM.

Furthermore, SDM systems employing Walsh carriers are less sensitive to noise than TDM systems. This is because noise is evenly distributed among all the multiplexed signals in a SDM system [16, p. 661].

The general principles of two methods of digital sequency multiplexing (DSM) using binary input signals will be outlined. In the first, each binary input signal amplitude modulates its assigned Walsh function, and the modulator outputs are combined in a linear summation process to produce a multi-level (M-ary) output.

In the second method, called binary DSM, the composite signal at the transmitter is passed through a slicer which has a binary (two state) output. This output is then transmitted in binary form and demodulated at the receiver.

Since analog methods of SDM have not been investigated in this project these will not be discussed.

3.3.2 MULTI-LEVEL DIGITAL SEQUENCY MULTIPLEXING

A MathCAD[1] simulation was used to determine the waveforms which will be encountered in the process of multiplexing and demultiplexing for different input data combinations. The operation of a system using four channels was explored in this way.

For the purpose of this simulation the Walsh functions were derived from Rademacher functions which, in turn, were derived from sinusoidal functions. The "IF" conditional was used to produce a set of square waves from the sinusoidal functions.

Modulator, and demodulator, outputs were taken as the product of the input signal and the corresponding Walsh carrier. Integration of each demodulator output gives an indication of the recovered data.

[1] MathCAD is owned by MathSoft, Inc. and the programme is copyrighted, with all rights reserved by MathSoft.

A simulation of the multi-level system of sequency division multiplexing using "MathCAD" is given in Appendix A.

3.3.2.1 Sequency modulation/multiplexing

A simplified block diagram of the multiplexer is given in Fig. 3.4. The system constructed makes provision for four data inputs.

Digital input signals, D_1, D_2, D_3, D_4, and the corresponding set of Walsh functions, $Wal(1,t), Wal(2,t), Wal(3,t), Wal(4,t)$, are applied to the modulators in each channel.

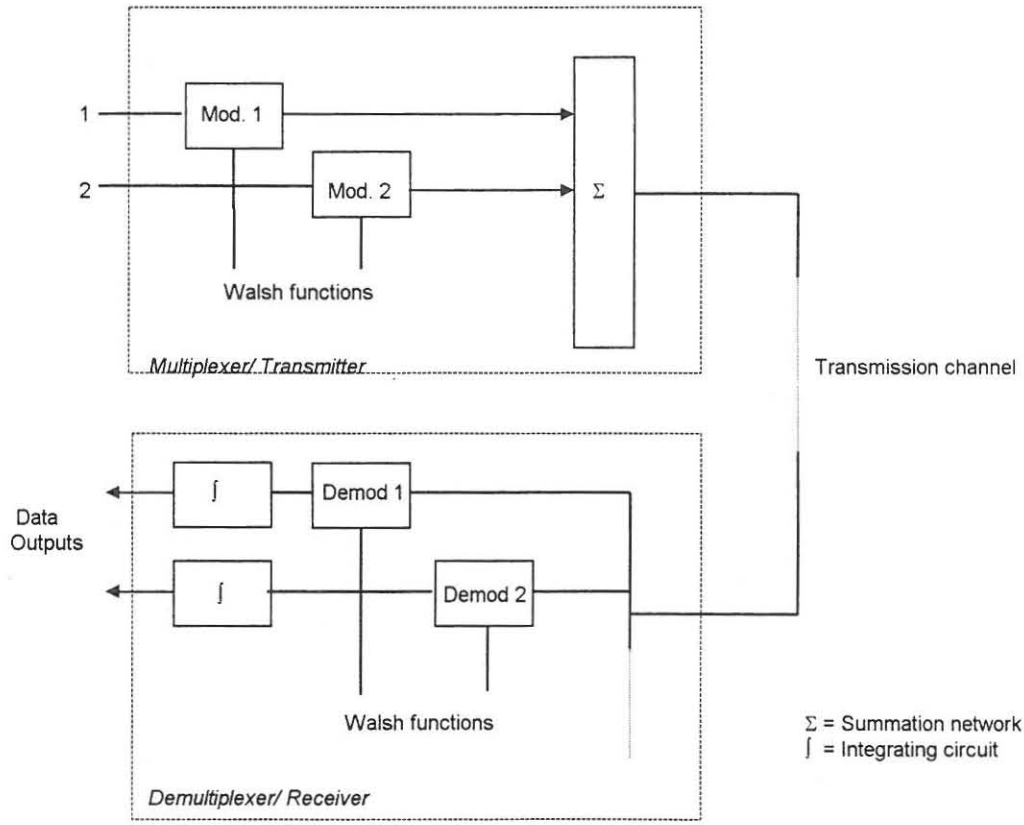


Fig. 3.4 *Block diagram of multi-level SDM system*

The Walsh carriers switch between +1 and -1 and are amplitude modulated by the binary input signals that have values of 1 or 0. A data input of 1 turns the modulator "on" and the Walsh carrier passes through to the output with amplitude +1 and -1. When the data input is 0, the modulator is turned "off" and the output is also 0. The action of the modulator is demonstrated by the truth table in Table 3.1

Table 3.1 *Sequency modulator truth table*

Data input	Walsh Carrier amplitude	Output
0	+1	0
0	-1	0
1	+1	+1
1	-1	-1

The modulator outputs are combined in a linear summing circuit and, if necessary, amplified before transmission across a common communication link to the remote receiver.

Digital data inputs must be synchronous with the Walsh functions.

The waveforms in Fig. 3.5 illustrate the action of the modulator/multiplexer circuits.

Typical digital input signals to the four channels are represented by the waveforms in Fig. 3.5(a), while Fig. 3.5(b) shows the Walsh carriers, and the modulator outputs are given in Fig. 3.5(c). The modulator outputs are combined in a linear summing circuit to produce the multi-level signal shown in Fig. 3.5(d).

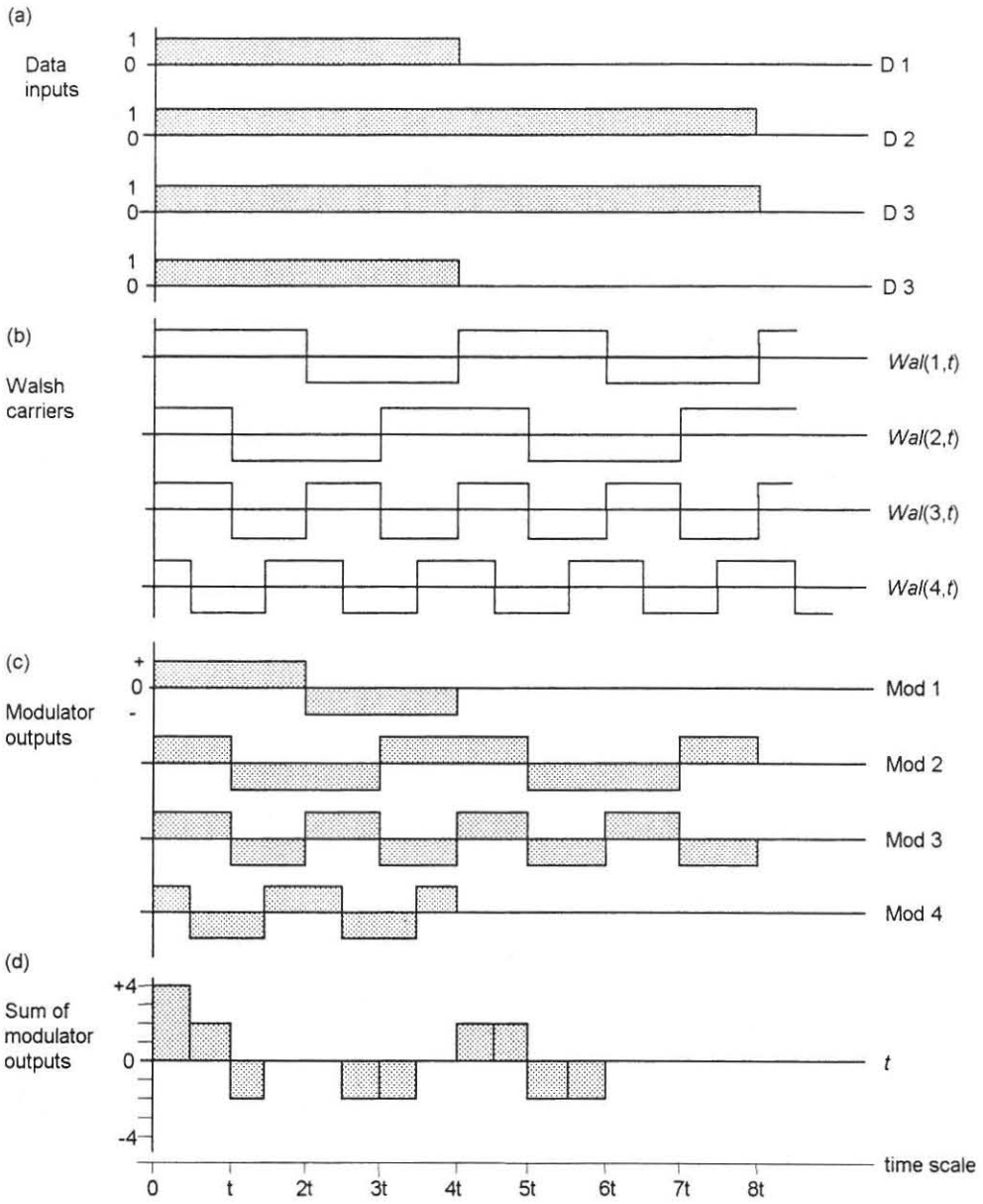


Fig. 3.5 *Waveforms of multi-level SDM system*

The four channel system produces octonary multi-level signals that have eight possible amplitude levels [10, p. 205].

3.3.2.2 Sequency demodulation/demultiplexing

The receiver is a correlating device of the form shown in Fig. 3.6.

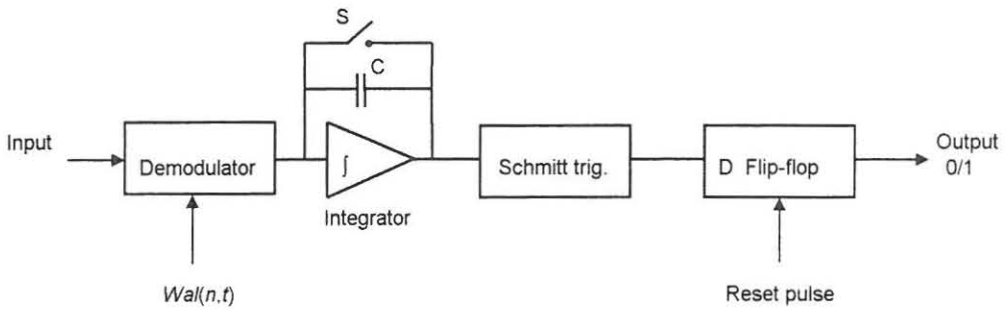


Fig. 3.6 *Block diagram of multi-level sequency demultiplexer*

Data in the four channels is separated by a process of synchronous correlation in the demodulator circuits where each multi-level signal is multiplied by a replica of the appropriate Walsh function for that channel.

The demodulator output in each channel is applied to an integrating circuit. The integrator output controls a Schmitt trigger which, together with a D flip-flop, determines whether a data 0 or 1 is present.

The output of each demodulator is a complex, multi-level signal as shown by the waveforms associated with *Wal*(1,*t*) in Fig. 3.7.

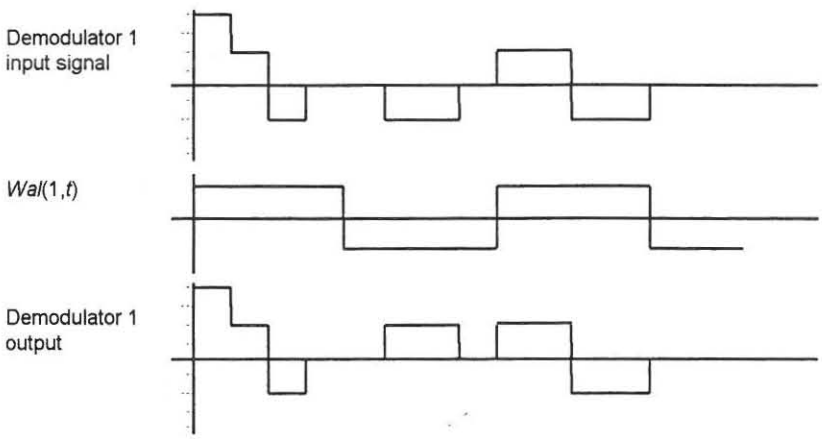


Fig. 3.7 *Output of multi-level sequency demodulator for a typical received signal*

Multiplying the demodulator input signal, point by point, with the corresponding Walsh function yields the output given in Fig. 3.7.

3.3.2.3 Data recovery filter

As shown by the receiver block diagram in Fig. 3.6, the output of each demodulator is applied to an integrating circuit. The integration process of the multi-level waveform and the action of the D flip-flop is illustrated in Fig. 3.8.

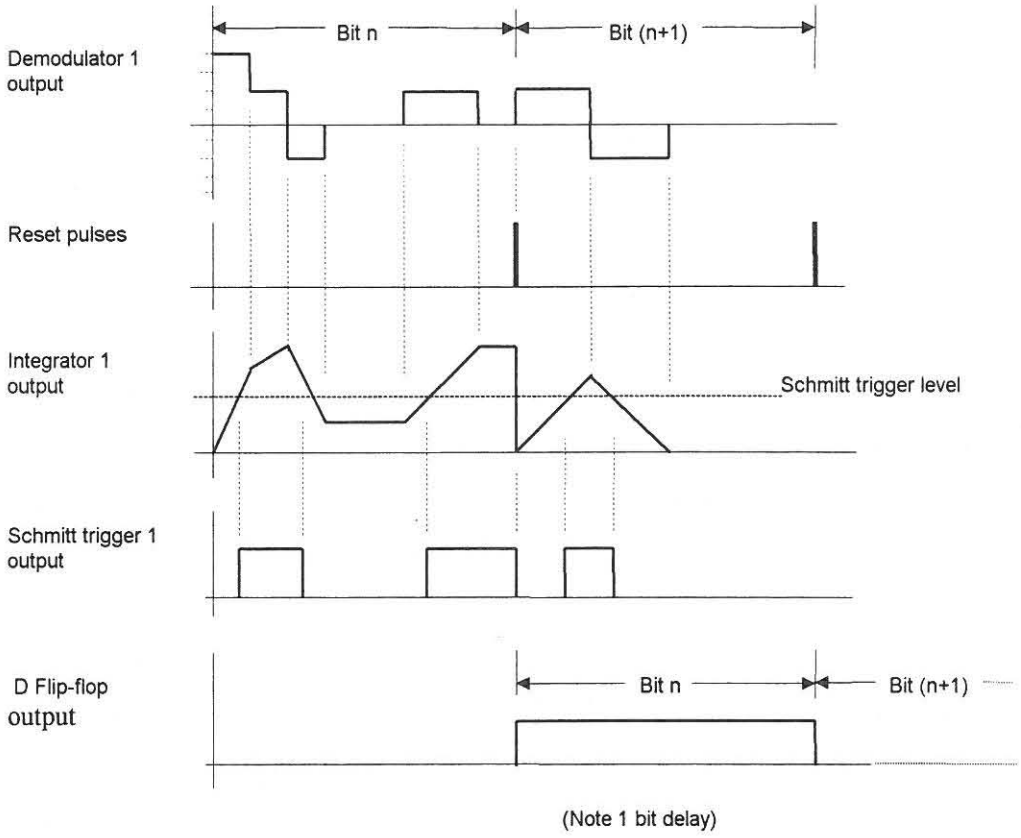


Fig. 3.8 *Integration of multi-level demodulator output signal.*

The integrating capacitor must be discharged by the switch *S* at the end of the integration period in order to reset the circuit in preparation for the next cycle of events.

The output of the integrator is passed on to a Schmitt trigger and a D flip-flop just before the integrating capacitor is discharged. This is done in order to decide whether a 1 or 0 data bit is represented at the integrator output. If the integrator capacitor voltage is below the trigger level of the Schmitt trigger, as indicated by the

broken line in Fig. 3.8, a logic "0" is passed on to the D flip-flop when a reset pulse occurs. Similarly, if the integrator output is above the trigger level, a logic "1" will be passed on.

As shown in Fig. 3.8, this decision process delays the system output by 1 data bit period.

3.3.3 BINARY DIGITAL SEQUENCY MULTIPLEXING

Multi-level signals have a variable peak-to-average power relationship and may readily be corrupted by noise. Such systems also require the use of very linear multipliers [2, p. 238].

Titsworth [25, p. 42], proposed a system in which the multiplexed output from the transmitter is a binary signal with only two amplitude levels.

Gordon and Barrett, [8, p. 417] constructed such an experimental system in which each codeword is scanned, timeslot by timeslot, and that character which is in the majority is taken as the signal which is to be transmitted.

The four channel system constructed for this project produces a binary signal in a different manner. The output from the linear summing circuit is sliced at a level determined by the combination of data at the input to the modulators.

The system constructed provides for four channels and uses the Walsh functions: *Wal (1,t), Wal (2,t), Wal (3,t), Wal (4,t)* as carriers.

3.3.3.1 Multiplexing/demultiplexing of binary DSM

A simplified block diagram of the binary DSM system is given in Fig. 3.9.

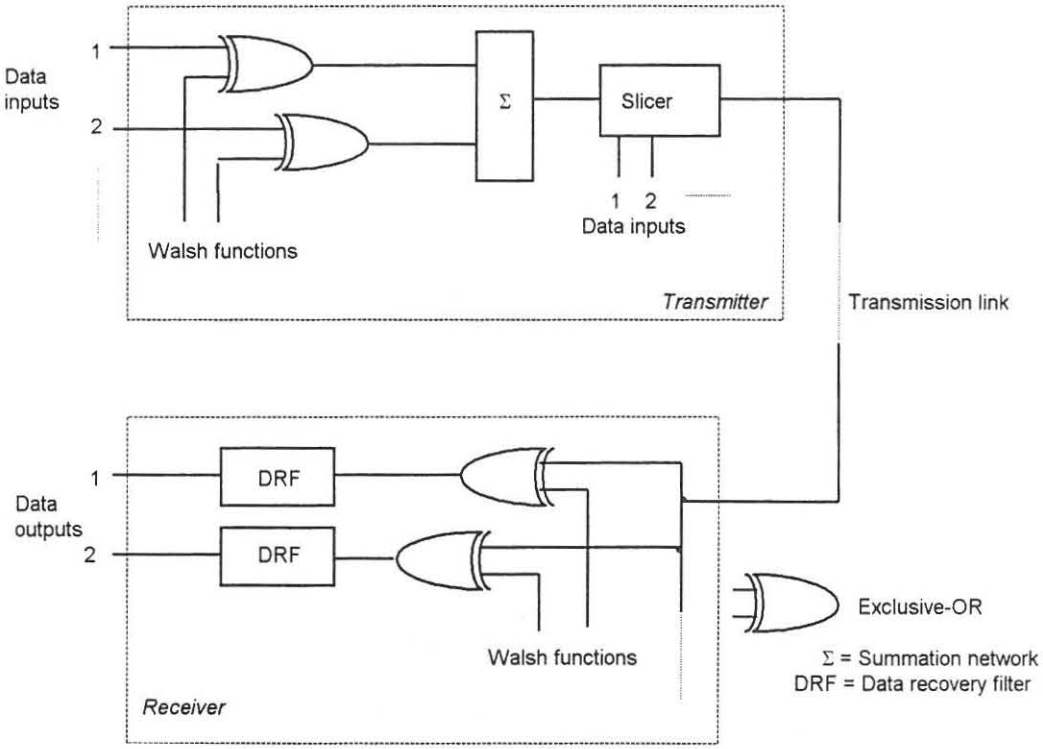


Fig. 3.9 *Block diagram of a binary SDM system*

Simple *exclusive*-OR logic was used to perform the function of modulation and demodulation. For this reason, the set of four Walsh functions that are used as carriers switch between +1 and 0, and not +1 and -1 as in the multi-level system.

The *exclusive*-OR modulator outputs are combined in a linear summing network and the composite signal is applied to the slicer.

By inspection of the waveforms it can be seen that if the output of the summing network is sliced at a fixed level the signal cannot be decoded correctly for all input data combinations. However, by setting the slicing level according to input data bits the original signals can be recovered at the receiver. The action of the slicer is discussed in section 3.3.3.2.

The slicer output consists of a series of binary pulses that is transmitted over the communications link to the remote receiver where *exclusive*-OR gates are used to demodulate the pulse train.

Integrator circuits are used with D flip-flops in the data recovery filters (DRF) to recover the original data.

As before, let the input data be synchronous with the set of truncated Walsh functions used as shown in Fig. 3.10.

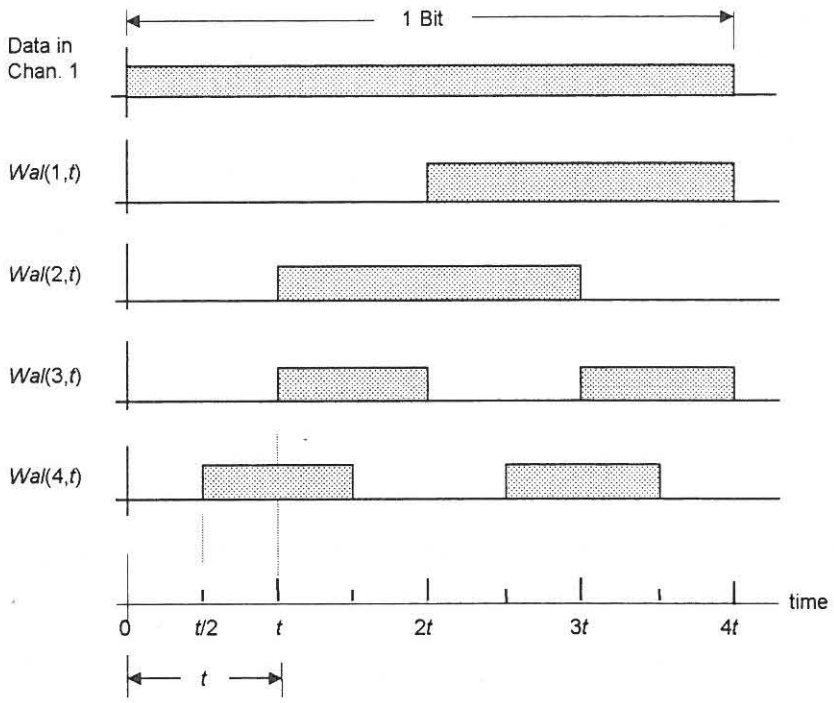


Fig. 3.10 *Waveforms of binary sequency division multiplexing*

The Walsh functions, $Wal(3,t)$, and $Wal(4,t)$, determine the width of the basic timeslot t as indicated in Fig. 3.10. It has been found that for reliable demultiplexing the duration of each data bit should not be less than four timeslots, t, as shown in Fig.3.10.[2]

The action of the *exclusive*-OR modulators is defined by the truth table in Table 3.2.

[2] See paragraph 4.1.4

Table 3.2 *Exclusive-OR truth table*

Data input	Walsh function	Exclusive OR output
0	0	0
0	1	1
1	0	1
1	1	0

The table shows that a "high" level output results only when the two inputs differ.

The timing of the waveforms of $Wal(3,t)$ and $Wal(4,t)$ is seen to differ by $t/2$, and hence the multi-level signal for each data bit in Fig.3.10 extends over a period of eight intervals of $t/2$.

3.3.3.2 Slicer

Four slicing levels, w, x, y and z are used as shown on the staircase multi-level signal in Fig. 3.11(a). The action of the slicer is depicted in Fig. 3.11(b). Here the typical multi-level signal shown is sliced at the second level, x, and is converted to a binary output signal with the aid of a comparator.

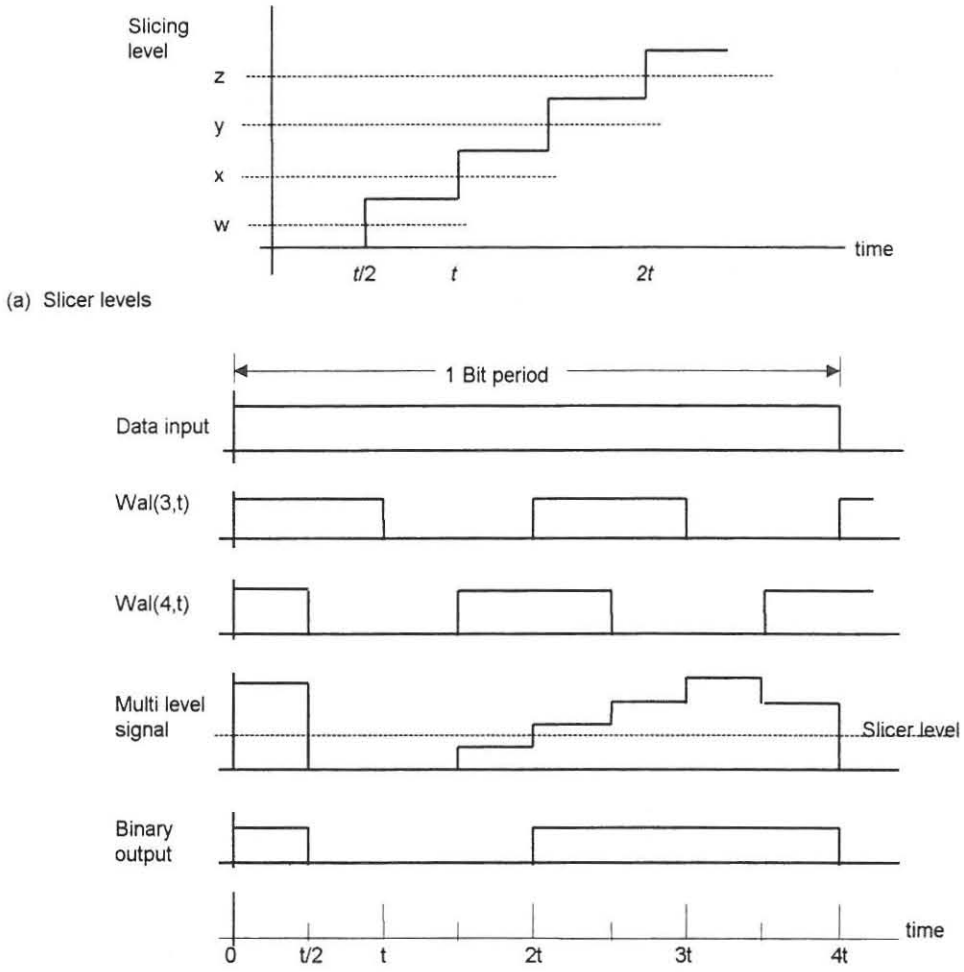


Fig. 3.11 *Slicing of the multi-level signal to produce a binary output*

The slicing level required for each combination of data inputs can be determined by inspection and proved experimentally. The optimum slicing levels found for reliable demultiplexing of various data inputs are given in Table 3.3.

A set of Boolean relations can be derived from this table and used to prepare a programmable array logic (PAL) circuit to accomplish the logic required for the slicing circuit.

Table 3.3 *Slicing levels used in four-channel DSM system.*

Data in a b c d	Slice level w,x,y,z	Data in a b c d	Slice level w,x,y,z
0 0 0 0	1	1 0 0 0	2
0 0 0 1	1	1 0 0 1	4
0 0 1 0	2	1 0 1 0	3
0 0 1 1	2	1 0 1 1	3
0 1 0 0	2	1 1 0 0	3
0 1 0 1	2	1 1 0 1	3
0 1 1 0	3	1 1 1 0	4
0 1 1 1	3	1 1 1 1	4

W = level 1, X = level 2, Y = level 3, Z = level 4

From the table;

$$w = \bar{a}\cdot\bar{b}\cdot\bar{c}\cdot\bar{d} + \bar{a}\cdot\bar{b}\cdot\bar{c}\cdot d$$

$$x = \bar{a}\cdot\bar{b}\cdot c\cdot\bar{d} + \bar{a}\cdot\bar{b}\cdot c\cdot d + \bar{a}\cdot b\cdot\bar{c}\cdot\bar{d} + \bar{a}\cdot b\cdot\bar{c}\cdot d + a\cdot\bar{b}\cdot\bar{c}\cdot\bar{d}$$

$$y = \bar{a}\cdot b\cdot c\cdot\bar{d} + \bar{a}\cdot b\cdot c\cdot d + a\cdot\bar{b}\cdot c\cdot\bar{d} + a\cdot\bar{b}\cdot c\cdot d + a\cdot b\cdot\bar{c}\cdot\bar{d} + a\cdot b\cdot\bar{c}\cdot d$$

$$z = a\cdot\bar{b}\cdot\bar{c}\cdot d + a\cdot b\cdot c\cdot\bar{d} + a\cdot b\cdot c\cdot d$$

3.3.3.3 Demodulation/demultiplexing

At the receiver the binary signals are demodulated with the corresponding Walsh functions. *Exclusive*-OR logic circuits are used for this purpose.

The output from each demodulator is also a binary signal that extends over eight periods of *t*/2 for each data bit.

Typical waveforms of the demodulation process are given in Fig. 3.12.

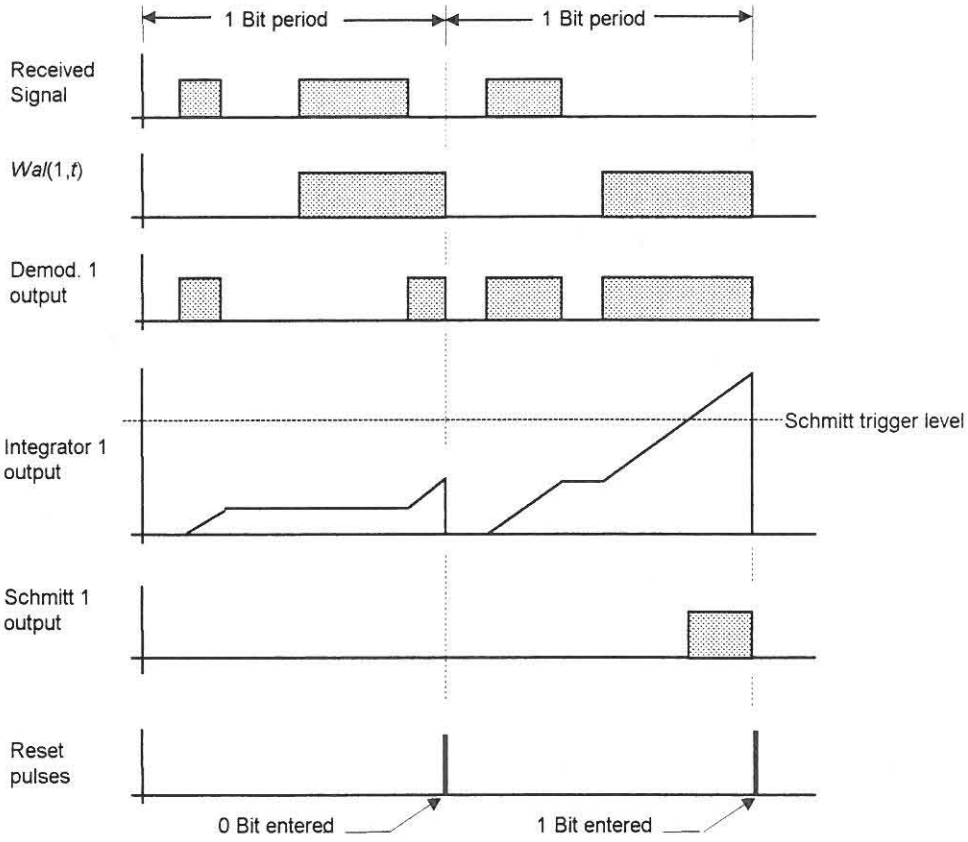


Fig. 3.12 *Demodulation of typical binary SDM signal*

3.3.3.4 Data Recovery Filter

As in the multi-level DSM system, the demodulator outputs are applied to a data recovery filter containing integrators, Schmitt triggers, and D flip-flops to recover the data bits. A typical output waveform from the integrator is shown in Fig. 3.12. The number of 1's in each interval of eight $t/2$ periods determines whether a data 1 or 0 has been received. The Schmitt trigger uses the integrator output at the end of the integrating period to establish a 1 or 0 condition.

In the system constructed, three or less 1's represent a 0 bit, while five or more 1's represent a 1 bit. The D flip-flop is set accordingly.

The complete process of multiplexing and demultiplexing for data inputs of 0 0 1 0 and 1 1 1 0 is depicted in Fig. 3.13.

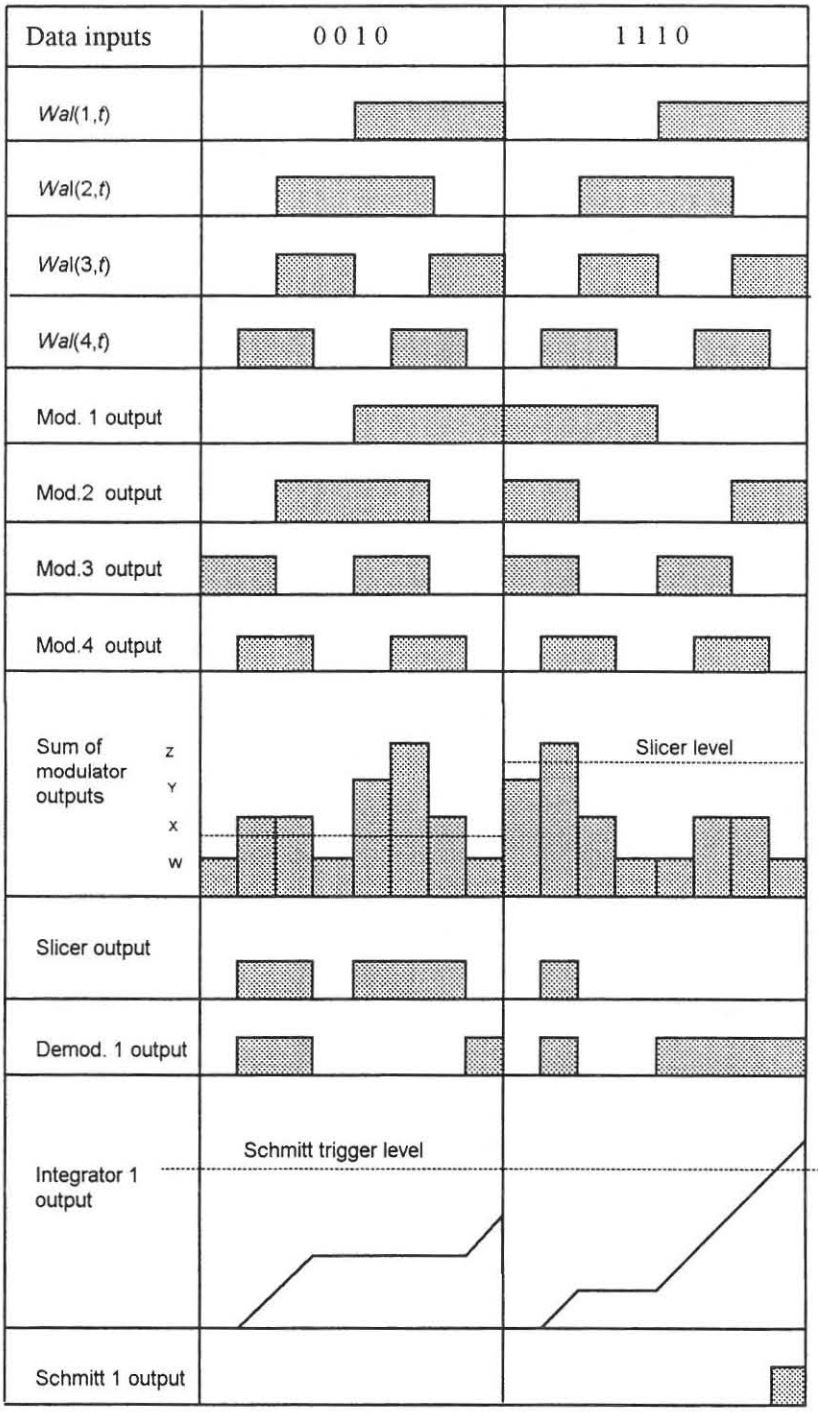


Fig. 3.13 *Principles of binary SDM for typical input data combinations*

When the data input to a particular modulator is at logic "0", the associated Walsh carrier passes through to the output without any change. However, when the data

input is at logic "1", the Walsh carrier is effectively inverted before passing through to the output.

The four data inputs, 0010, are applied to the *exclusive*-OR modulators 1, 2, 3 and 4 together with the Walsh carriers: *Wal(1,t), Wal(2,t), Wal(3,t), Wal(4,t).*

The modulator outputs are combined and sliced as shown before transmission as binary signals.

Demodulator 1 output is given in Fig. 3.13. The output from the demodulator is integrated and then applied to a Schmitt trigger which determines whether a "1" or "0" bit has been received.

3.4 DC SHIFT

The influence of dc shift due to changes in component values or incidental dc signals on the communications link on the performance of the system has not been investigated. However, it is anticipated that as the data recovery filter measures the integrator output signal amplitude against the trigger level of a Schmitt trigger that errors will occur.

3.5 SUMMARY

* With frequency division multiplexing each baseband signal is modulated onto a different carrier so that the sidebands occupy different parts of the frequency spectrum. Band-pass filters must be used to select the required sidebands.

* Time division multiplexing samples each input at least at the Nyquist rate of $2.f_m$. The samples are transmitted one after another and are separated by a switching arrangement at the receiver.

* In Multi-level sequency division multiplexing, each data input modulates a Walsh function. The outputs of all the modulators are combined to produce

a multi-level signal which is then transmitted. At the receiver the multi-level signal is multiplied by replicas of the Walsh carriers in demodulator circuits. The demodulator outputs are applied to data recovery filters where the original data signals are recovered.

* In Binary sequency division multiplexing the signals that are transmitted to line have only two levels viz 0 and 1. These binary signals are demodulated by multiplication with the Walsh functions, and passed through data recovery filters as in the case of multi-level SDM.

* The sequency division multiplexing system used has an inherent 1 bit delay.

Chapter 4

IMPLEMENTATION OF SEQUENCY DIVISION MULTIPLEXING

4.1 DESCRIPTION OF THE MULTI-LEVEL SYSTEM

The multi-level system of sequency division multiplexing which has been constructed is described in section 4.1.1 to 4.1.9.3 , while details of the binary system of sequency division multiplexing are given in section 4.2.1 to 4.2.5.

4.1.1 SIMPLIFIED BLOCK DIAGRAM

A multi-level sequency division multiplexing (SDM) system consisting of the necessary transmitting and receiving equipment for the parallel transmission of four-bit binary words was constructed for experimental purposes.

Four channels were provided to cater for parallel transmission of the four-bit words. Alternatively, the four channels can be used for serial transmission of four separate data streams.

A short length of cable was used to carry SDM signals from the transmitter to the receiver. This simple link can be opened to facilitate the insertion of test equipment such as a noise generator, filter and amplifier/attenuator in the transmission path of the multi-level SDM signals.

Since carrier recovery at the receiver was not part of the requirements for this project, a common generator output was used for the Walsh carriers at both the transmitter and the receiver.

Both analog and digital circuit techniques were used, and hence the power requirements were; +5 volt, +7,5 volt and -7,5 volt. Power for the circuits was obtained from analog and digital breadboard training units[1].

[1] E & L Instruments, Inc.

The basic layout of the equipment is illustrated by the simplified block diagram in Fig. 4.1.

Input data to each of the four channels is applied to the modulators, together with the appropriate Walsh functions. The outputs of the modulators are combined and passed along the transmission link to the receiver.

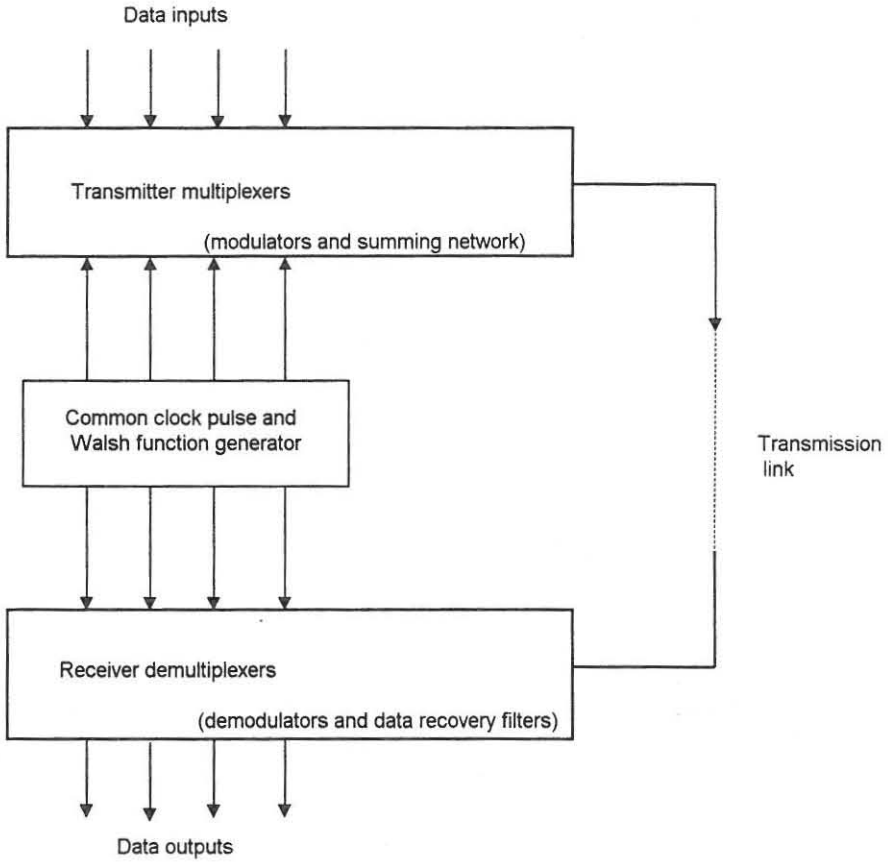


Fig. 4.1 *Simplified block diagram of four-channel SDM system*

The transmitter (multiplexer) consists of four modulators with a linear summing network to combine the modulator outputs.

At the receiver the multi-level SDM signals and the relevant Walsh functions are applied to the demultiplexer circuits where the original data is recovered and separated into the four channels.

The receiver (demultiplexer) consists of four demodulator circuits, with four data recovery filters. Each data recovery filter has an integrating circuit, a Schmitt trigger and a D flip-flop.

The clock pulse and Walsh function generator contains a crystal oscillator with frequency dividing and counter circuits to produce the set of four Walsh functions which are used as carriers.

The system was designed for the transmission of digital data at a rate of 1 200 bits per second in each channel but can readily be altered to work at lower or higher data rates.

4.1.2 DATA INPUT AND WALSH CARRIERS

The Walsh functions used as carriers are; *Wal*(1,*t*), *Wal*(2,*t*), *Wal*(3,*t*) and *Wal*(4,*t*). Waveforms of these carriers have been given in chapter 3, Fig. 3.5, to demonstrate the process of modulation.

The amplitude of each of the Walsh function carriers produced by the Walsh function generator switches between 0 volt and + 3,5 volt. The modulator circuits have been designed to work directly with these carrier inputs. However, the demodulator circuits at the receiver require Walsh carrier inputs that switch between + 1,5 volt and - 1,5 volt. A Walsh function amplifier is used to provide the correct amplitude and reversal of potentials of the waveforms.

The data input signals are nominally + 5 volt for a logic "1", and 0 volt for a logic “0”.

The minimum number of zero crossings of the Walsh carriers that are necessary for each data bit is most important for reliable signalling and this topic is discussed further in section 4.1.4.

The most significant bit (MSB) is applied to channel 1 modulator together with its carrier *Wal*(1,*t*). Similarly, the least significant bit (LSB) and its carrier, *Wal*(4,*t*), are applied to channel 4 modulator.

4.1.3 FUNCTIONAL BLOCK DIAGRAM

A more detailed block diagram of the Walsh function generator, multi-level sequency division multiplexer and the demultiplexer, is given in Fig. 4.2.

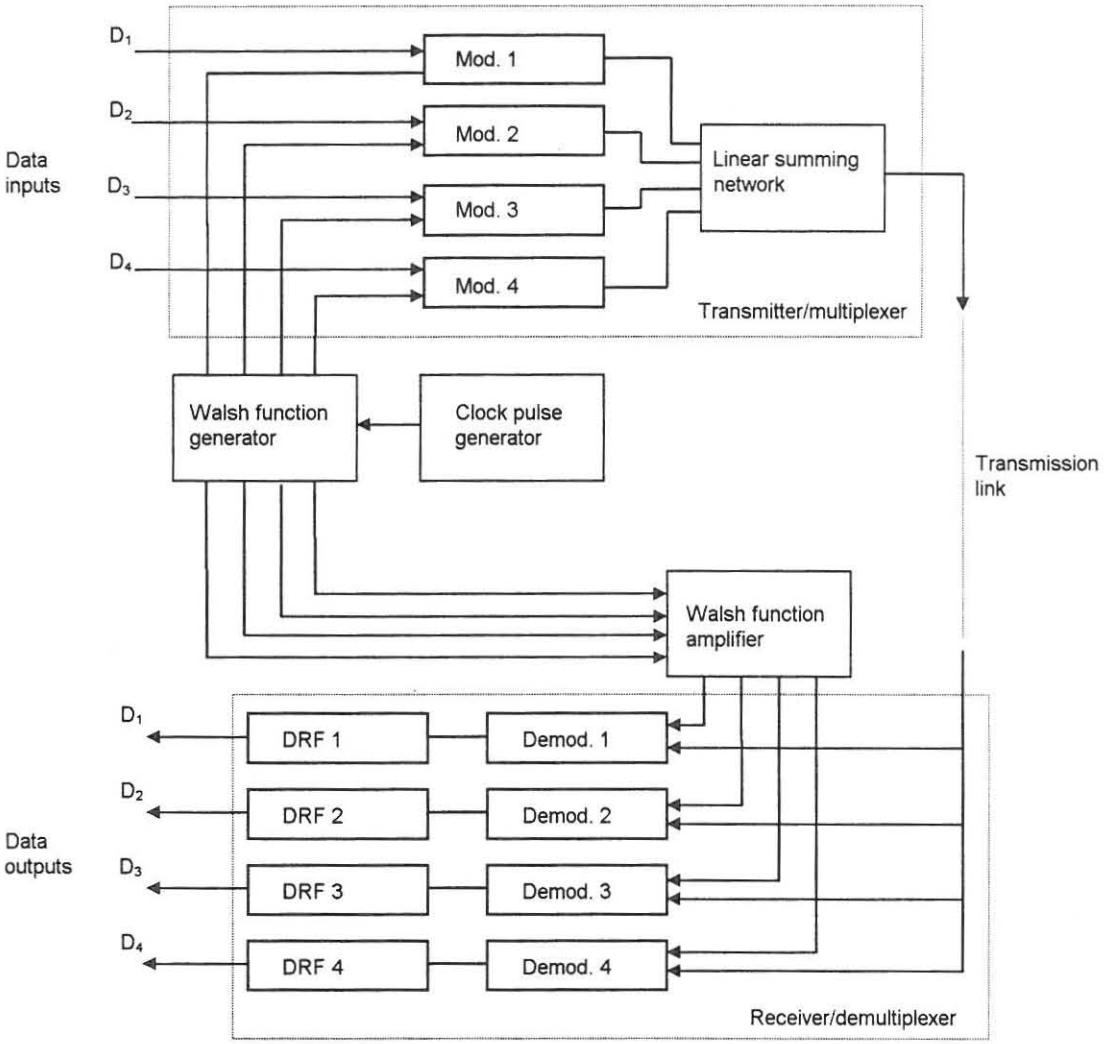


Fig. 4.2 *Functional block diagram of four channel multi-level SDM system*

The clock pulse generator (CPG) and Walsh function generator (WFG) are used to produce a continuous train of Walsh carriers, *Wal*(1,*t*), *Wal*(2,*t*), *Wal*(3,*t*) and *Wal*(4,*t*). These Walsh carriers are applied to the modulator and demodulator circuits.

Because of the abrupt transitions between the 0 volt and + 3,5 volt carrier levels, "glitches" were introduced into the modulator circuits and were present on the output signals. The glitches were disposed of by connecting small capacitors of 6,8pF between the outputs and inverting inputs of the operational amplifiers in the modulator circuits. Screened wire was used for the signal lines and care was taken to avoid earth loops in the construction of the circuits.

Data signals at each of the four channel inputs modulate the respective Walsh carriers. The modulator outputs are combined in a simple summing network to produce the multi-level SDM signal which is then transmitted.

At the demultiplexer, the received multi-level SDM signals are applied to four demodulators, together with replicas of the Walsh carriers used in the multiplexer. In each of these demodulators the received signal is "multiplied" by it's respective Walsh carrier.

The output of each demodulator is a complex, multi-level signal. Typical multi-level output signals of the demodulators are given in Fig. 4.3 for a received signal representing the four bit word (1 1 1 0).

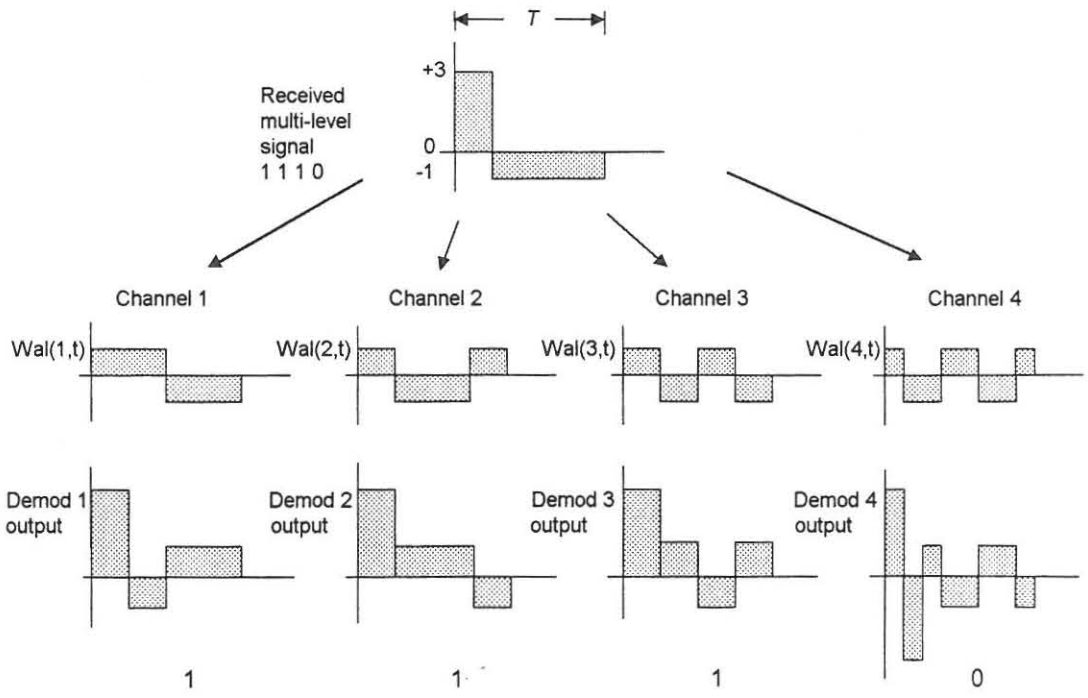


Fig.4.3 *Typical multi-level demodulator output signals for data inputs of* 1 1 1 0

The output of each demodulator is then applied to a data recovery filter (DRF) in order to recover the original train of 1's and 0's in each channel.

Each section of the multi-level SDM equipment is discussed separately in chapters 4.1.5 to 4.1.9.3.

4.1.4 RELATION OF BIT PERIOD TO CARRIER TIME-FRAME

In this section the Walsh functions are sometimes referred to as "codewords" [25, p. 42].

The experimental system constructed was designed for a signalling speed of 1 200 bits per second in each channel. The question then arises "what should be the relationship between the data rate and the sequency (no. of zero crossings per second) of the Walsh carriers ?"

Consider the set of Walsh carriers (codewords) *Wal(i,t)* defined on an interval [0,T] as in Fig. 4.4. The period, *T*, is referred to as the "frame time" [22, p. 318], and *i* is the index, or order, of the function.

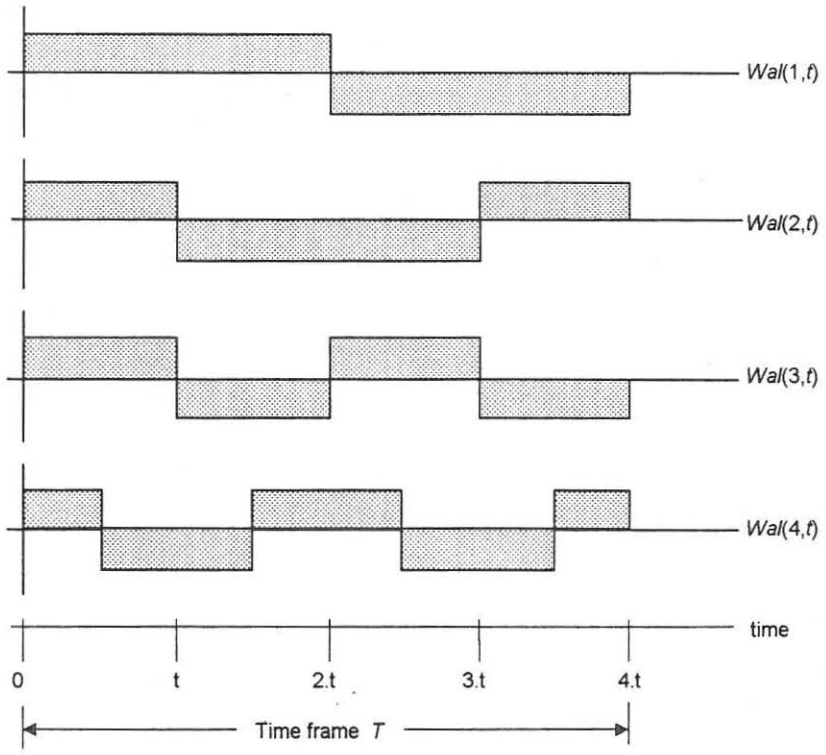


Fig. 4.4 *Time-frame of Walsh functions*

In this set of functions the frame time is given by one complete period of *Wal*(1,*t*). The number of characters contained in the highest order function is 4, and therefore the frame time, *T*, contains 4 characters.

As discussed in section 3.3.2.1 the action of each modulator in the multiplexer is such that when a data input of "1" is applied to it, it allows the carrier to pass through. A data input of "0" turns the modulator off and its output is zero.

Provided that the input data bits have a duration of an integral number of time frames the modulator output waveforms will satisfy the conditions for orthogonality given in section 2.2 and the multi-level signal will be successfully decoded by the receiver demodulators.

However, if the length of the codewords used as carriers is less than one time-frame there will be loss of orthogonality and crosstalk will result between the channels.

This situation is illustrated in Fig. 4.5 for the four channel system using codewords with a length of one half a time-frame, ie; $L = T/2$.

While the system will work for several combinations of data inputs with carrier codewords of less than one time-frame, it fails on other combinations producing severe crosstalk between the channels.

In the example shown in Fig. 4.5 a data input bit of "1" is applied to channel 2 only. The data inputs to the other channels are considered to be at "0". Modulator 2 output is then the waveform that is transmitted over the communications link to the receiver.

Output waveforms of the demodulator and integrator circuits are given for all four channels for a data input of "1" in channel 2 only. From these it can be seen that the integrator outputs of channels 1 and 4 are zero at the end of the time, $T/2$, but that the integrator outputs of channels 2 and 3 are both "high" at the end of the time frame producing outputs of "1" in both these channels, although the output of channel 3 should be "0".

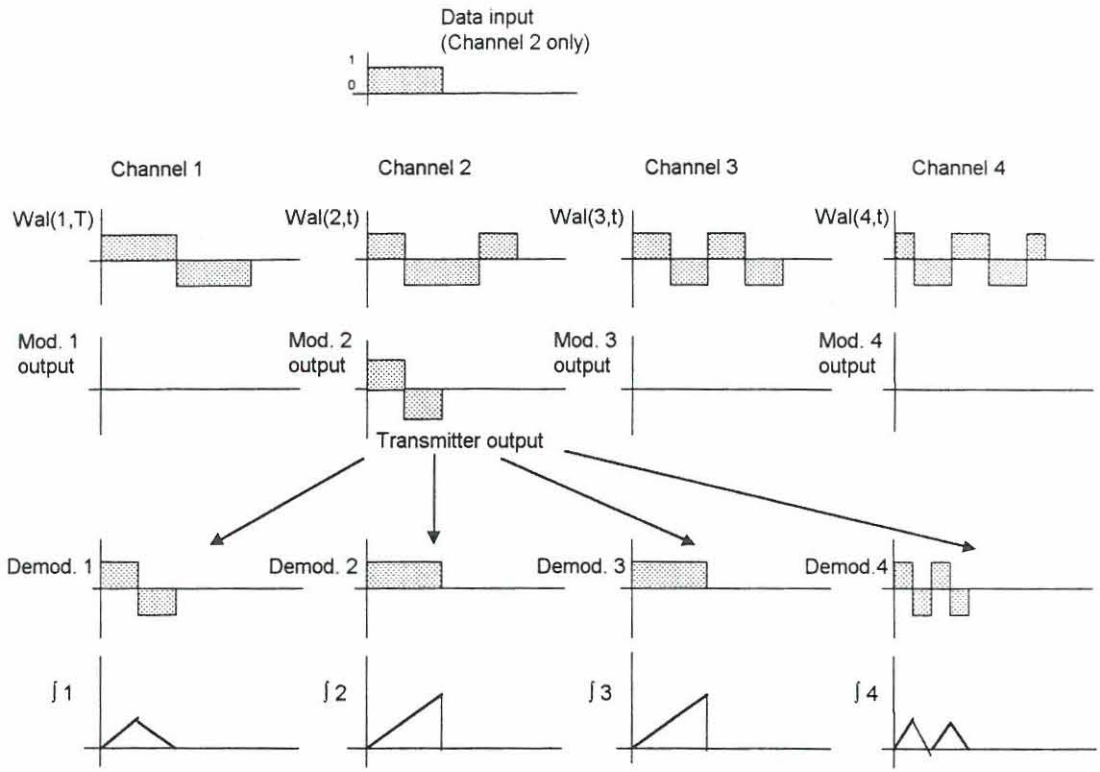


Fig. 4.5 *Transmission of data with codewords of less than one time-frame*

Titsworth [25, p. 44] suggests that codewords with a length of $L = 2^n$ should be used to minimise crosstalk between channels, where n refers to the number of channels. Hence, a four channel system would require a word length of 16 characters per data bit. If the signalling speed of 1 200 data bits per channel is maintained, and the word length of the Walsh carriers is increased according to $L = 2^n$ the frequency spectrum of the signals will be increased accordingly, as well as the bandwidth requirements of the system.

Gordon and Barrett [8, p. 418] devised a computer programme to determine suitable Walsh carriers for a given codeword of length $L = n$, where n refers to the number of channels used. Using the results obtained they employed the Wash functions; $Wal(1,t)$, $Wal(2,t)$,.....$Wal(7,t)$ with a codeword length corresponding to the time-frame of these functions to assemble a seven channel sequency multiplexing system. This system required that an odd number of channels should be used.

The four channel system which was constructed for this project also used a codeword length of one time-frame of the Walsh functions for each data bit. This corresponds with the period of *Wal*(1,*t*). The number of characters in this period is given by *Wal*(4,*t*) as 4. Then; $L = n$.

This is in line with the basic multi-level system described by Schreiber [22, p. 332] in which the bit time of the signal word corresponds exactly with the Walsh function carrier period" and is significantly less than the standard suggested by Titsworth as described previously.

The system constructed was tested using codewords of length $L = \frac{3T}{4}$ and $L = \frac{T}{2}$. In both cases the crosstalk between channels was found to be unacceptably high.

However, it was found that reliable transmission of data can be achieved with codewords of length $L = T$.

If the bit period is increased to a multiple of one time-frame there will be built-in redundancy with better noise immunity. Consider, for example, using a codeword length of $L = 2T$. In effect this would be the same as sending each data bit twice!

4.1.5 CLOCK PULSE GENERATOR

The clock pulse generator (CPG) employs a 6,144 MHz crystal oscillator to provide an accurate and stable means of generating the Walsh function carrier waveforms. Two modulo 16 counters, and one decade counter, are used in the arrangement shown in Fig. 4.6 to divide down to the required clock frequency.

The output of the 6,144 MHz oscillator drives the first modulo 16 circuit which produces a square wave output at a frequency of 6,144/16 MHz = 384 KHz. The 384 kHz waveform is applied to a decade counter which has an output of 38,4 KHz. This is in turn passed on to a second modulo 16 counter from which outputs of 2,4 KHz, 4,8 KHz, 9,6 KHz and 19,2 KHz are obtained.

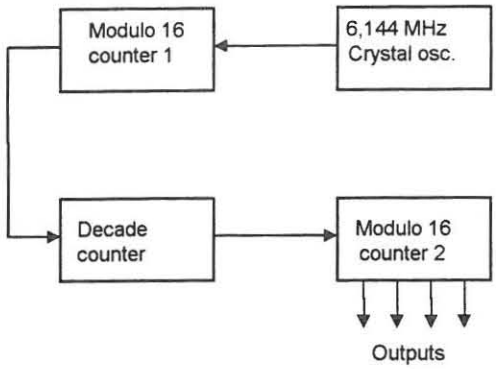


Fig. 4.6 *Block diagram of the clock pulse generator*

The complete circuit arrangement of the clock pulse generator is given in Fig. 4.7. Integrated circuits, IC 1, IC 2, IC 3 and IC 4 all operate from the + 5 volt supply.

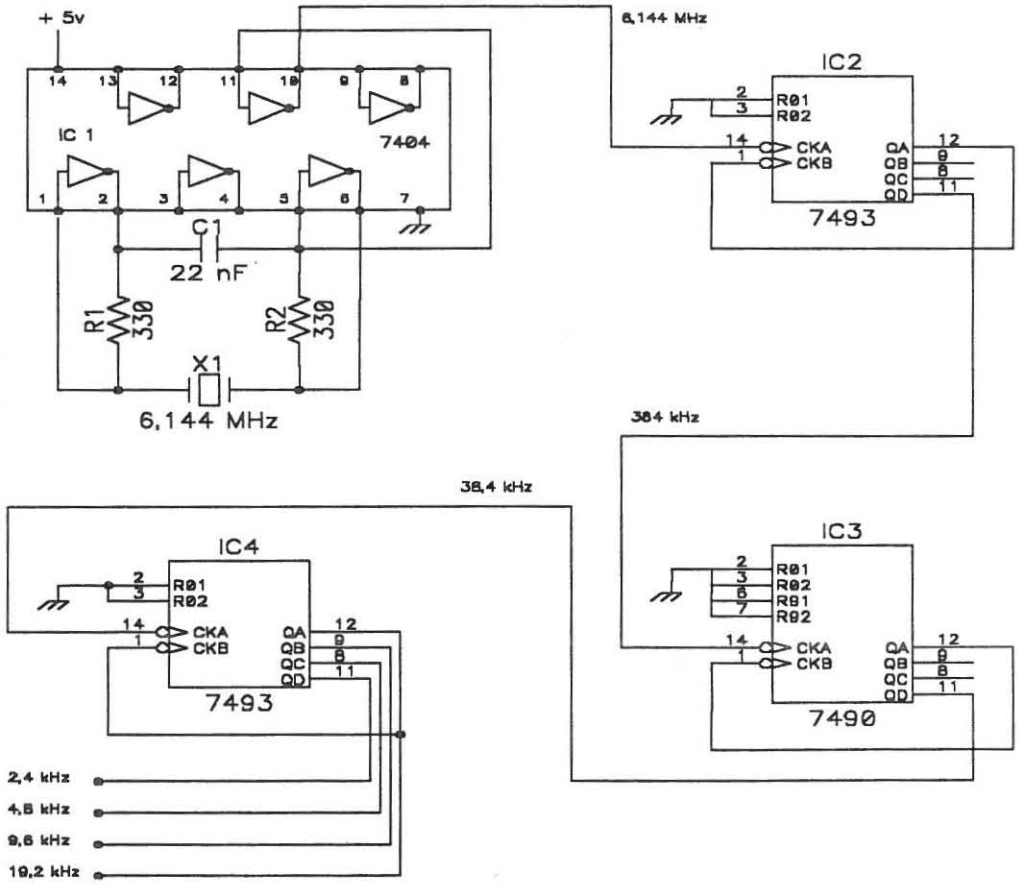


Fig. 4.7 *Clock pulse generator circuit*

A 7404 TTL hexadecimal inverter integrated circuit is used in a conventional crystal oscillator circuit [17, p. 28].

Inverters 1 and 3 were connected as a two stage amplifier with a 22 nF coupling capacitor between them. The 330Ω resistors in the feedback path of each inverter are used to set the gain of the inverting amplifiers. A 6,144 MHz crystal connected in the feedback path from invertor 3 output on pin 6, to inverter 1 input on pin 1 determines the frequency of oscillation of the circuit. Inverter 5 was used as a buffer amplifier producing a stable 6,144 MHz square wave output at pin 10.

The 6,144 MHz crystal oscillator output drives a conventional modulo 16 circuit [7, p. 79]. The 7493 integrated circuit contains four J-K flip-flops with outputs Q_0, Q_1, Q_2, Q_3. Each flip-flop has a clock pulse (CP) input. The clock inputs to Q_0 and Q_1, ($\overline{CP_0}$ and $\overline{CP_1}$), are externally accessible on pins 14 and 1 respectively. Each flip-flop has a clear input connected to the output of a NAND gate with two inputs, MR_1 and MR_2. As these were not used in this application they were connected to ground.

The circuit was used as a ripple through counter that completes it's cycle of events after every 16 input pulses. The J-K flip-flops produce outputs of 3,072 MHz, 1,536 MHz, 768 kHz and 384 kHz.

A 7490 integrated circuit was used as a binary coded decimal (BCD) counter that completes it's cycle of events after every 10 input pulses [7, pp. 84-85]. The circuit contains four flip-flops that can be arranged as a BCD counter by connecting output Q_0, to the input, $\overline{CP_1}$, of flip flop 1. The 384 kHz output from the first modulo 16 circuit is applied to the input, $\overline{CP_0}$ of the decade counter. The frequency of the output at Q_3, is 38,4 kHz.

A second modulo 16 circuit was used to further divide down the decade counter output of 38,4 kHz to produce outputs of 19,8 kHz, 9,6 kHz, 4,8 kHz and 2,4 kHz. [7, p.79].

The outputs of the counter were wired to pins on the circuit board which may be connected, as required, via jumper leads to the Walsh function generator circuits.

Veroboard construction was employed for the construction of all the circuits once the design of each had been finalised on "Digi-designer" boards.

4.1.6 WALSH FUNCTION GENERATOR

The four carriers, *Wal*(1,*t*), *Wal*(2,*t*), *Wal*(3,*t*) and *Wal*(4,*t*), required for the modulator and demodulator circuits are produced by the Walsh function generator. The unit pulse method described below was used to generate the series of Walsh functions required [2, pp. 140-142]

4.1.6.1 Unit pulse generator

A unit pulse generator using the principle of added-pulse generation was employed as the Walsh function generator. The block diagram arrangement in Fig. 4.8 shows the principle of operation of the unit-pulse method of Walsh function generation.[2]

In this circuit a ring counter using a 74164 TTL integrated circuit eight-bit shift register is employed to produce a set of block pulse functions. The block pulses are combined in "OR" gates as required for the Walsh functions. At this stage the Walsh functions switch between the "0" and "1" states.

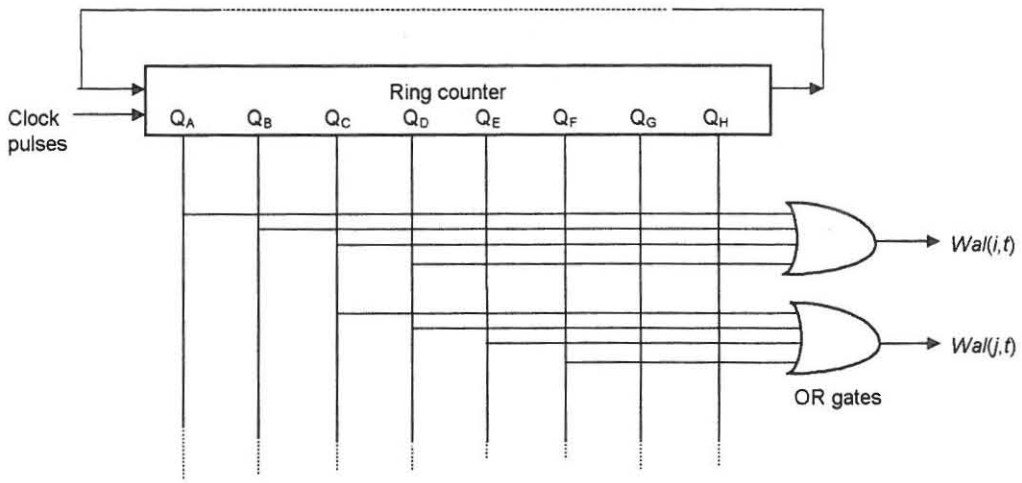


Fig. 4.8 *Principle of operation of the unit-pulse Walsh function generator*

[2] See paragraph 2.6.4

The shift register moves a single “1” from one flip-flop to the next through the counter under the control of clock pulses. As the “1” progresses from one stage to the next it switches the output of each stage, Q_A, $Q_{B,}$, ...Q_H, in turn to the “1” level, and back to zero again, as it passes on. The set of output waveforms are known as "block pulses".

The circuit arrangement of the unit pulse Walsh function generator is given in Fig. 4.9.

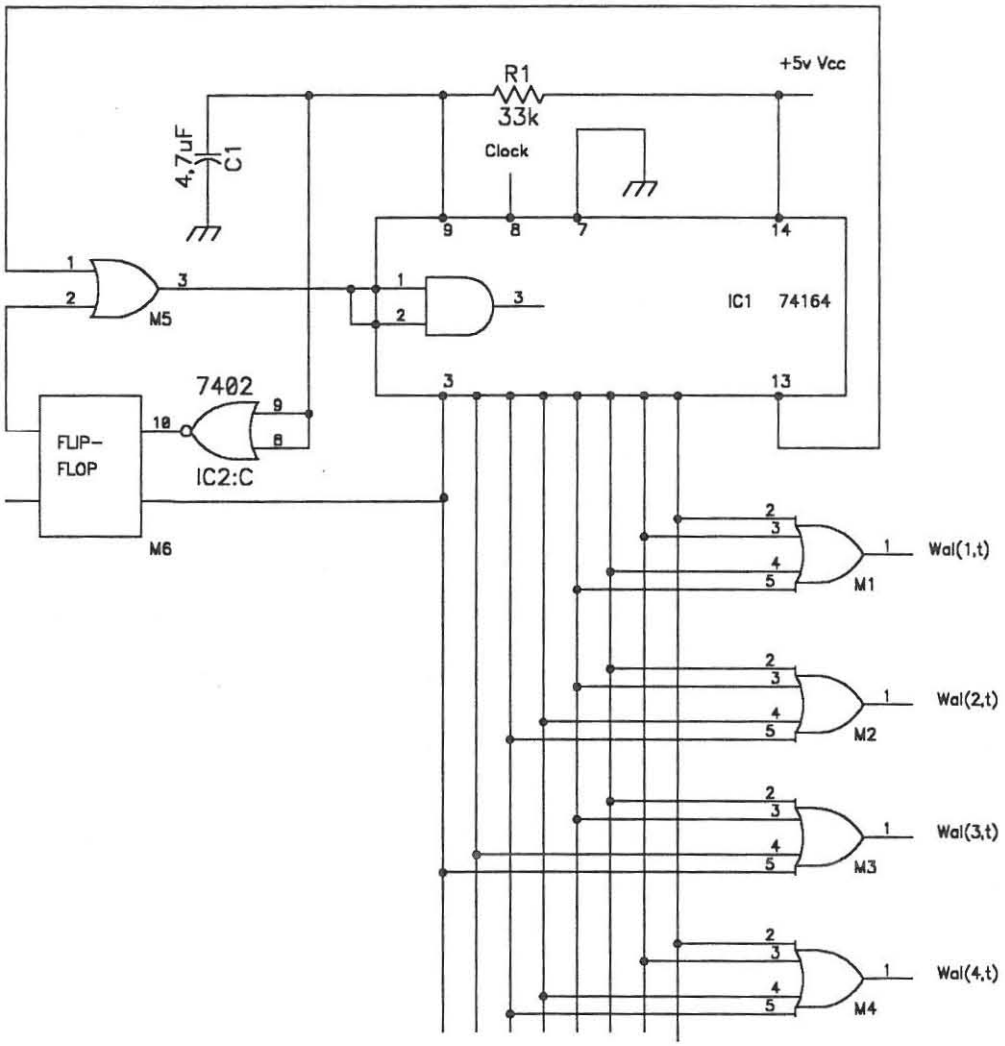


Fig. 4.9 *Circuit arrangement of unit-pulse Walsh function generator*

In order to produce the required waveforms, a single logic "1" must progress through the counter under the control of clock pulses. The counter circuit must preset automatically when power is applied to ensure that only a single "1" bit is present.

The power-on reset circuit shown in Fig. 4.9 employs R_1 and C_1 for this purpose [17, pp. 321-322].

The capacitor C_1 has no initial charge when power is applied to the circuit and the voltage across it at pin 9 of the IC is zero. Hence a "0" condition is applied to the counter to reset all the flip-flops. The capacitor voltage rises exponentially to the power supply potential of + 5 volt at a rate determined by the values of C_1 and R_1.

When power is applied to the shift register circuit, the transient in the power-on circuit is inverted by a simple 7402-gate arrangement and is used to *set* the R-S flip-flop (module 6).

This causes the output of the OR gate (module 5) to be "1", and the first transition shifts the "1" into flip-flop Q_A. When Q_A output goes high it resets the external flip-flop. At this stage Q_A contains a "1" and all the other flip-flops within the 74164 shift register are at "0". The inverter output remains low while power is on and the R-S flip-flop does not change state.

Output pulses from Q_H (pin 13) pass through the OR gate to the input, AB, at pins 1 and 2. In this way a "1" bit is clocked around the shift register circuit.

The internal arrangement of modules 5 and 6 is given in Fig. 4.10.

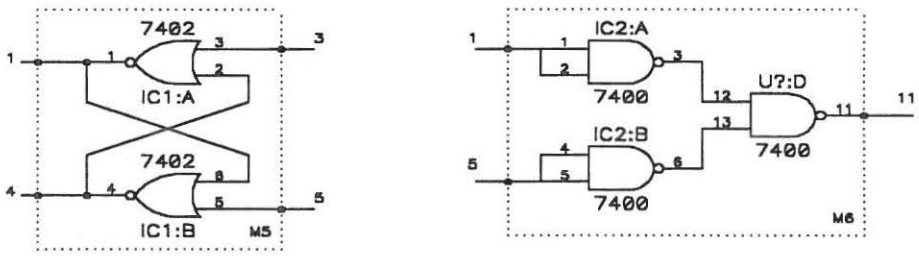


Fig. 4.10 (a) *Module M6. NOR gates connected as R-S flip-flop*
(b) *Module M5. NAND gates connected as OR gate*

Conventional "NOR" logic was used for the R-S flip-flop with inputs at terminals 3 and 5, and outputs at terminals 1 and 4.

Similarly, an "OR" gate was built using a set of 7400 "NAND" gates.

The block pulse output waveforms from Q_A, Q_B ..... Q_H from the unit-pulse generator are given in Fig. 4.11.

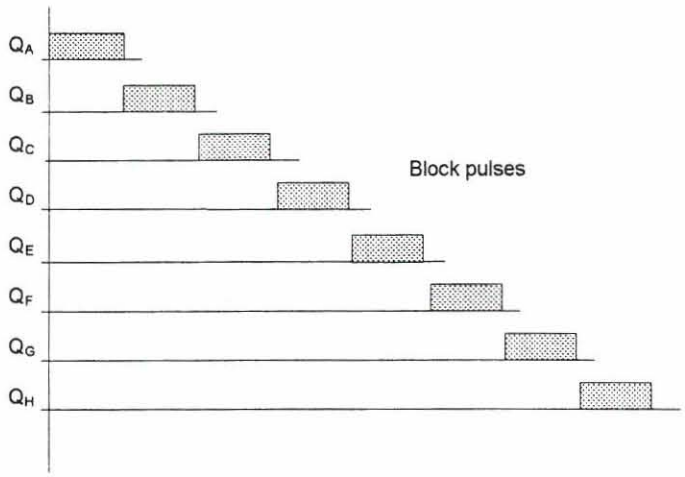


Fig. 4.11 *Block pulses produced by the unit-pulse generator*

Different combinations of the block pulses are combined in a set of logic gates to produce the set of Walsh functions required. The block pulse waveforms are combined by the four-input logic circuit arrangement shown above in Fig. 4.9.

The eight output lines from the unit-pulse generator are connected by jumper leads to the combining circuits to produce the required Walsh functions.

Table 4.1 Shows the combinations of block pulses which have been used to obtain the Walsh functions.

Table 4.1 *Use of shift register outputs to produce Walsh functions*

	BLOCK PULSES							
Walsh function	A	B	C	D	E	F	G	H
Wal(1,*t*)					x	x	x	x
Wal(2,*t*)			x	x	x	x		
Wal(3.*t*)	x	x			x	x		
Wal(4,*t*)	x			x	x			x

The added pulse method of Walsh function generation has proved to be very flexible for this application as other codeword combinations are readily obtained simply by altering the jumper lead connections.

4.1.6.2 Walsh function amplifier

The Walsh functions obtained from the TTL combining circuits switch between 0 volt and +3,5 volt. These logic levels are directly suitable for use with the modulator.

The amplifier circuit in Fig. 4.12 is used to alter the logic levels in such a way that logic "1" is at +7,5 volt, and logic "0" at -7,5 volt so that the sequency signals switch symmetrically about the zero level. Operational amplifiers with FET inputs have been used in the linear circuits [6, pp. 40-52].

The logic levels are altered by combining a dc component with the input signals at W1, W2, W3 and W4. Provision is made for both inverted and non-inverted outputs. The amplitude of the dc component is set by RVI to obtain an output that is symmetrical about the zero axis[3].

[3] The voltages of the +7,5 volt and -7,5 volt power supplies must be correctly set before attempting to adjust RV1.

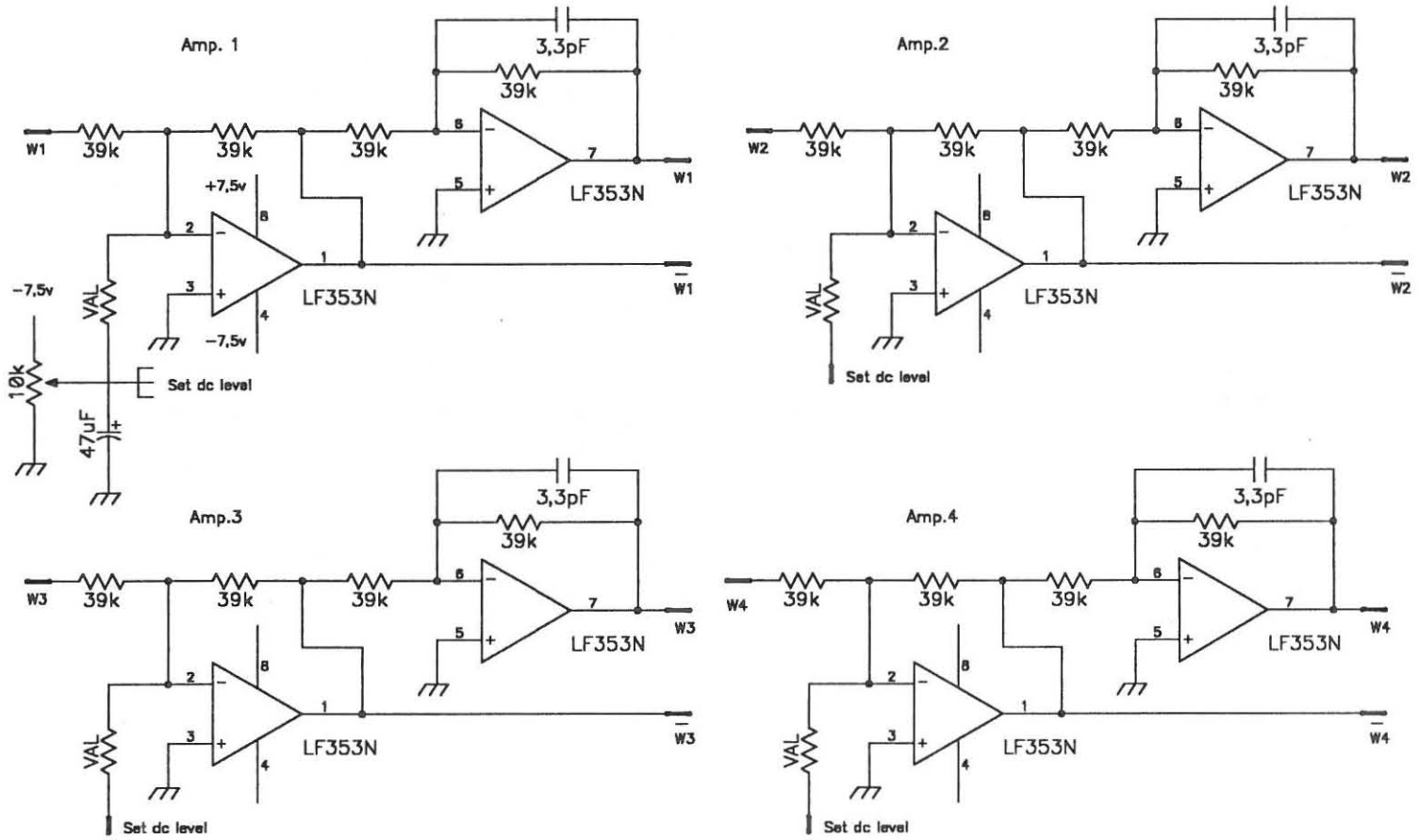


Fig. 4.12 *Walsh function amplifier*

4.1.7 SEQUENCY MULTIPLEXER

Binary data input signals must amplitude modulate the Walsh functions. When the data input is at "0", the modulator output must also be zero. However, when the data input is at logic "1" the associated Walsh function must pass through to the output and produce a signal that switches between +7,5 V and -7,5 V. From this it is seen that the modulator circuit must produce three output levels, viz; +7,5 V, 0V, and - 7,5 V.

In order to satisfy this requirement it was necessary to make use of analog circuit techniques together with digital circuitry.

4.1.7.1 Sequency modulator

Elements of the single channel modulator circuit which was used are given in Fig. 4.13. The circuit consists of a 7408 TTL "AND" gate, a 7400 TTL "NAND" gate used as an inverter, and an LF 353 operational amplifier.

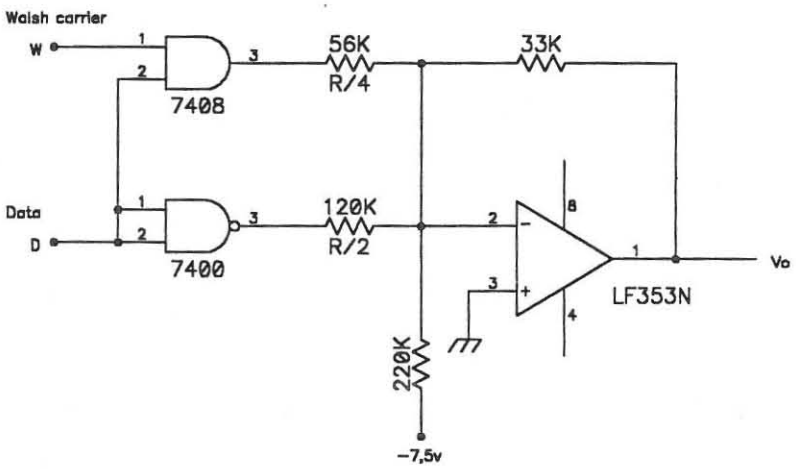


Fig. 4.13 *Basic Walsh function modulator circuit*

Boolean expressions for the digital part of the circuit may be written as:

$S = \overline{D}$ (this signal will control the dc level shift)

$R = D \cdot W$ (This is effectively the product of the Data and Walsh function inputs indicating that modulation takes place).

Where:

D = Data input

W = Walsh function input

S = Output of the 7400

R = Output of the 7408

The action of the circuit may be explained with reference to the waveforms in Fig. 4.14

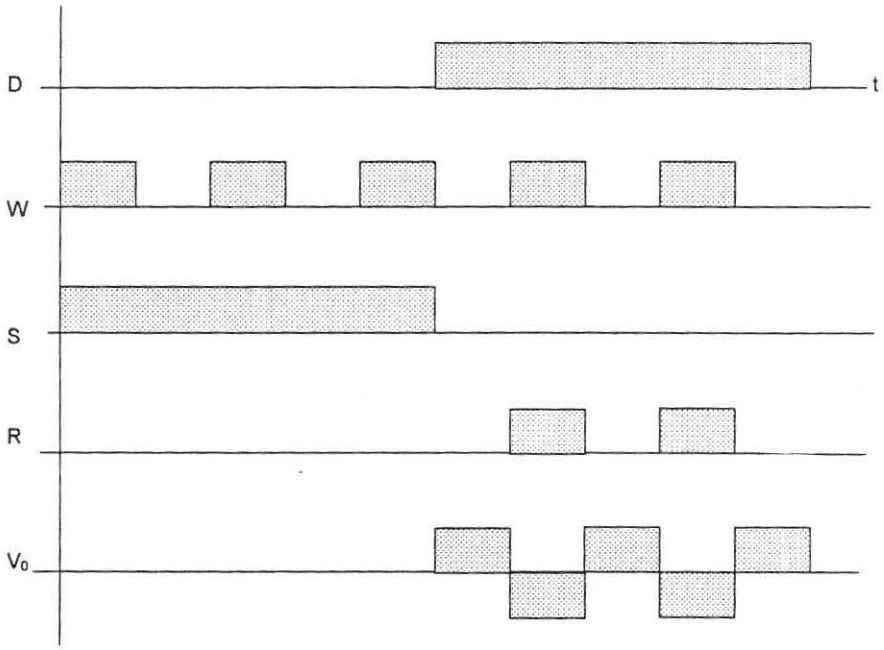


Fig. 4.14 *Action of the Walsh function modulator with typical input signals*

The data signal itself acts as an "enable" signal which allows the Walsh carrier to pass through the 7408 "AND" gate when the data input is at "1", and closes off this circuit when the data input is at 0.

This is the "AND" function in which *R* = *D.W.* The circuit is required to act in such a way that the output will be zero when the data input is "0", and switch between +7,5v and -7,5v under the control of the Walsh function carrier when the data input is at "1".

The data input signal can be used to provide a "level" shift during the presence of a modulated signal.

When the data input is "0", S = "1". This potential, combined with that from the -7,5 volt supply at the inverting input of the operational amplifier, provides a bias such that V_O = 0 volt.

When the data input is "1", S = 0. Only the bias from the -7,5 volt supply is present and it shifts the level of the modulated signal as in Fig. 4.14, producing an output V_O which switches between +7,5 V and -7,5 V.

The action of the modulator circuit is summarised in Table 4.2.

Table 4.2: *Truth table of Walsh modulator circuit*

D	*W*	*R*	*S*	V_0
0	0	0	1	0
0	1	0	1	0
1	0	0	0	1
1	1	1	0	-1

It is seen that three output levels result, viz "1", "-1" and "0".

4.1.7.2 Summing circuit

Four Walsh modulators are used in this multiplexing arrangement and their outputs must be combined in a linear summing circuit.

A conventional operational amplifier summing circuit is used for this purpose, and it's circuit diagram is given in Fig. 4.15.

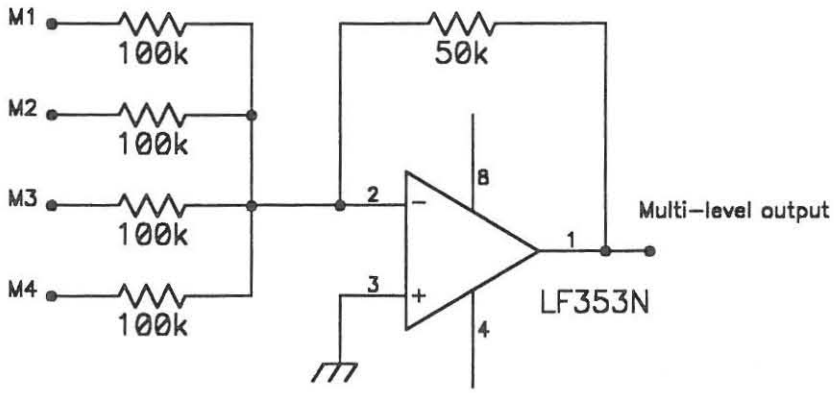


Fig. 4.15 *Modulator output summing circuit*

The complete circuit diagram of the four channel Walsh function modulator with the summing circuit is given in Fig. 4.16.

The 1K potentiometer, RV1, must be adjusted to produce a 0 volt output when all the data inputs are made "0".

The Walsh function modulator forms the basis of the four channel multi-level sequency division multiplexer.

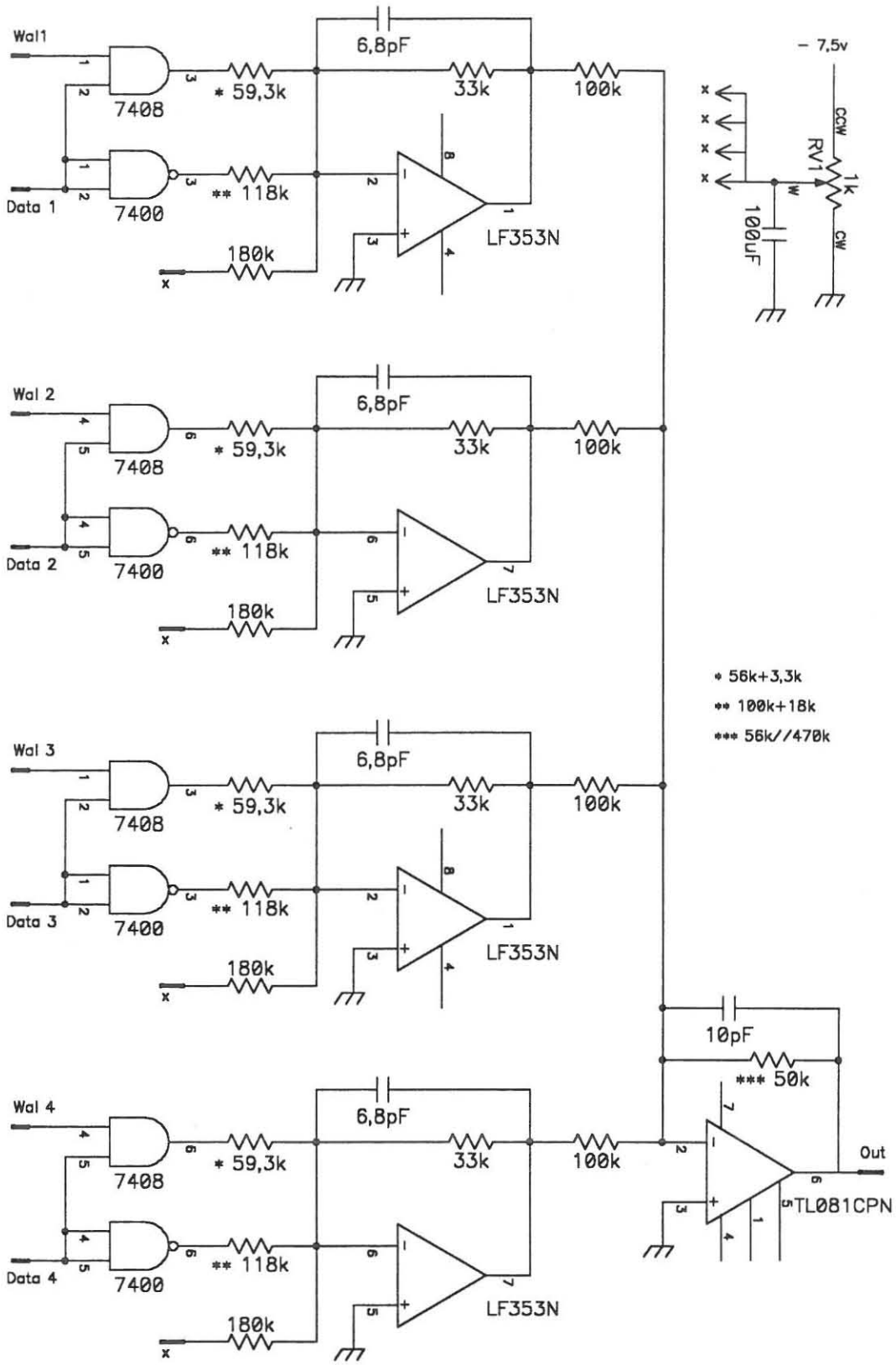


Fig. 4.16 *Four-channel Walsh function modulator and summing circuit*

4.1.8 SEQUENCY DEMULTIPLEXER

4.1.8.1 Demodulators

At the receiver the four channel multi-level signals are separated out into their respective channels by a process of demodulation in which the received signals are multiplied by the relevant Walsh function in each demodulator.

A linear multiplying circuit is required to obtain the product of the received multi-level signal and the associated Walsh function in each channel [10, p. 205]. The circuit shown in Fig. 4.17 was used as a demodulator.

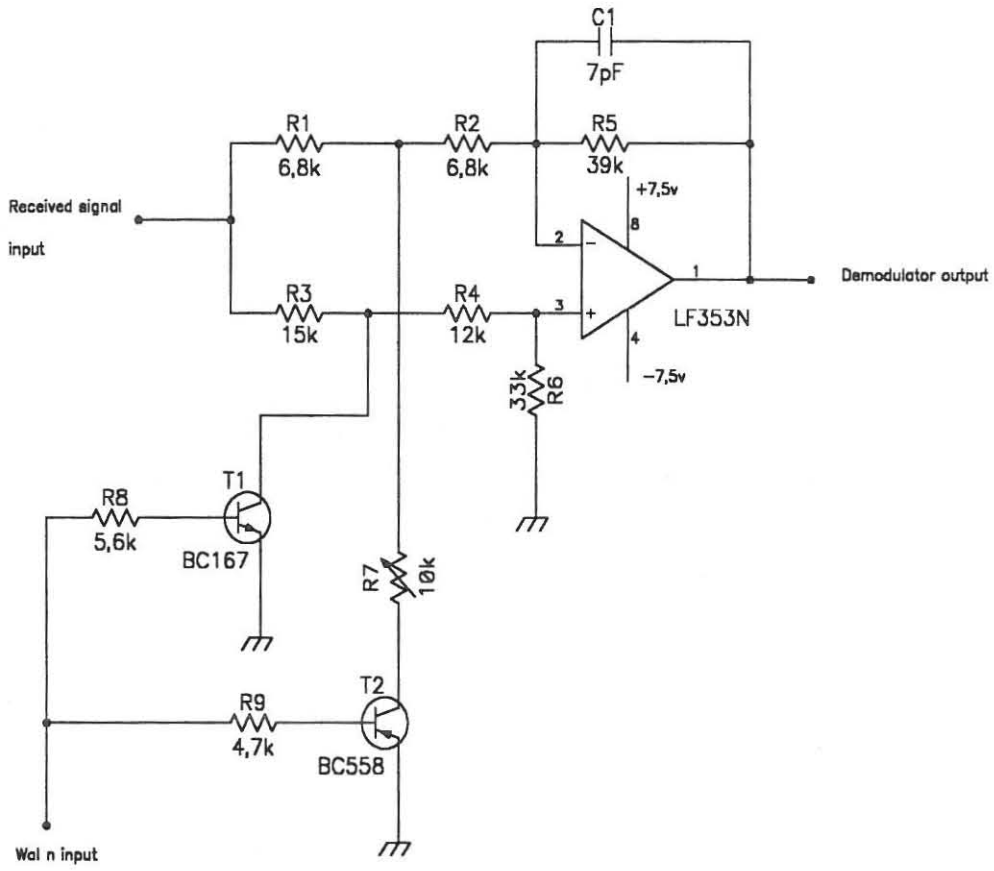


Fig. 4.17 *SDM demodulator*

The received signal is applied to both the inverting and non-inverting inputs of the differential amplifier.

R1, R2, R3, R4 are proportioned in such a way that the output of the amplifier is zero when the Walsh function carrier is not present. Resistor R7 is used to compensate for differences in reverse saturation and leakage currents in the transistors T1 and T2.

The Walsh function carrier turns the transistors T1 and T2 on and off alternately shorting the inverting and non-inverting inputs to earth. These transistors operate in both the standard and inverse modes as the polarity of the received signal reverses.

For example, consider the condition when the polarity of the received signal is positive wrt earth. During the time that the Walsh carrier is positive it turns T1 on and biases T2 off. The non-inverting input is shorted to earth and the amplifier output will be negative.

When the carrier becomes negative it biases T1 off and turns T2 on. The roles of the collector and emitter of T2 are reversed and the inverting input is shorted. Under these conditions the amplifier output will be positive.

Now assume that the polarity of the received signal reverses such that it is negative wrt earth. When the Walsh carrier is positive it turns T1 on and T2 off. Transistor T1 conducts in the inverse mode and shorts out the non-inverting input and the amplifier output will be positive. When the carrier is negative transistor T1 is turned off and T2 is on. The inverting input will be shorted and the amplifier output is negative.

Turning transistors T1 and T2 on or off during the time that the received signal is zero will have no effect and the amplifier output will be zero.

From the above it can be seen that the output of the demodulator is inverted. For this reason the $\overline{Wal}$ outputs of the Walsh function amplifiers are used to correct the polarity of the demodulator outputs.

The action of the demodulator for channel 2 is explained with reference to the waveforms in Fig. 4.18. Here it is seen that the demodulator is supplied with $\overline{Wal(2,t)}$.

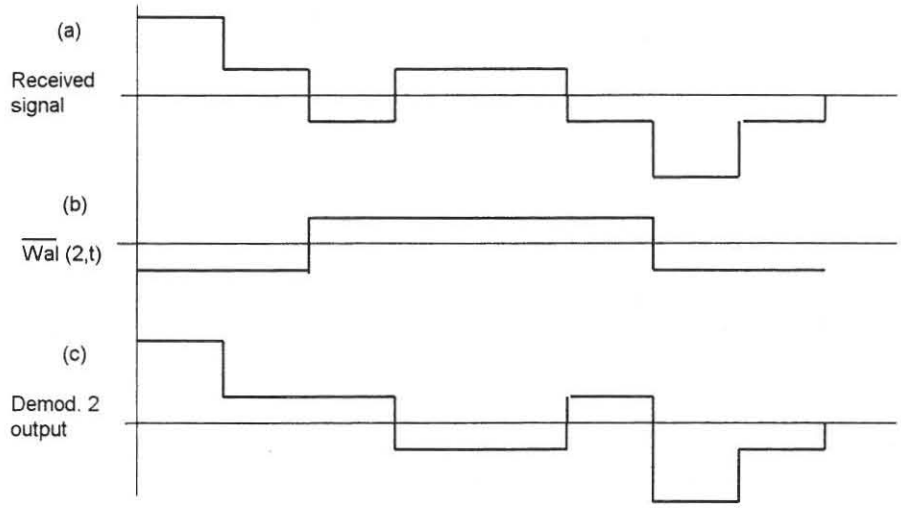


Fig. 4.18 *Demodulation of a typical multi-level signal*

The waveform of a typical multi-level SDM signal, representing data inputs of 1011, is shown at (a) in Fig. 4.18. The Walsh carrier for channel 2 is given by (b), and the demodulator output at (c).

Although the demodulator output is a complex multi-level waveform, it's average value will be positive if a "1" data bit is present in that particular channel. The average value of the demodulator output will be zero, or close to zero, if a "0" is received in the channel.

The complete circuit arrangement of the four channel demodulator is given in Fig. 4.19.

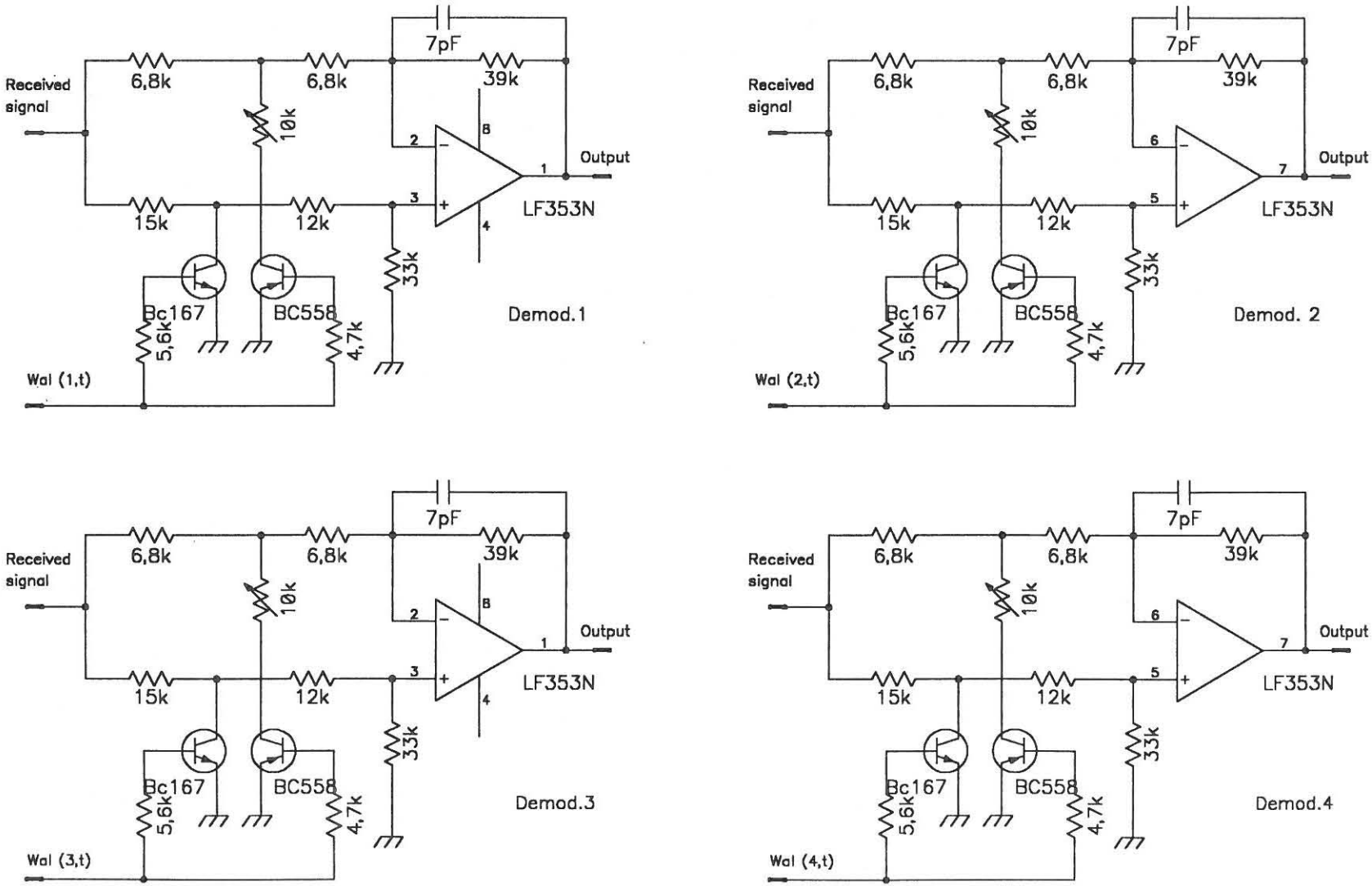


Fig. 4.19 *Four channel demodulator*

4.1.9 DATA RECOVERY FILTER

A data recovery filter is used to recover the stream of data bits from the complex demodulator output waveform in each channel. The general block diagram arrangement of the data recovery filter is given in Fig. 4.20.

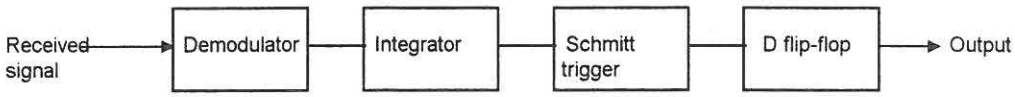


Fig. 4.20 *Block diagram of data recovery filter.*

The average height of the demodulator output must be examined in each data bit interval to determine whether a "1" or "0" bit has been received.

For this purpose each channel contains an integrator and an output circuit with a Schmitt trigger and a D flip-flop.

The integrator circuit "smoothes" the demodulator output waveform and at the end of each data bit interval it is reset to zero by momentarily shorting the integrating capacitor.

The integrator output is applied to a Schmitt trigger which switches whenever the integrator output voltage exceeds a certain level. If the output of the Schmitt is "high" when a reset pulse arrives the D flip-flop is toggled producing a "1" at the channel output.

The action of the data recovery filter is illustrated by the typical waveforms in Fig. 4.21. The received signal represents a data input of 1101.

Since the D flip-flop is triggered at the end of the integrating period it's output will be delayed by one data bit relative to the input data stream.

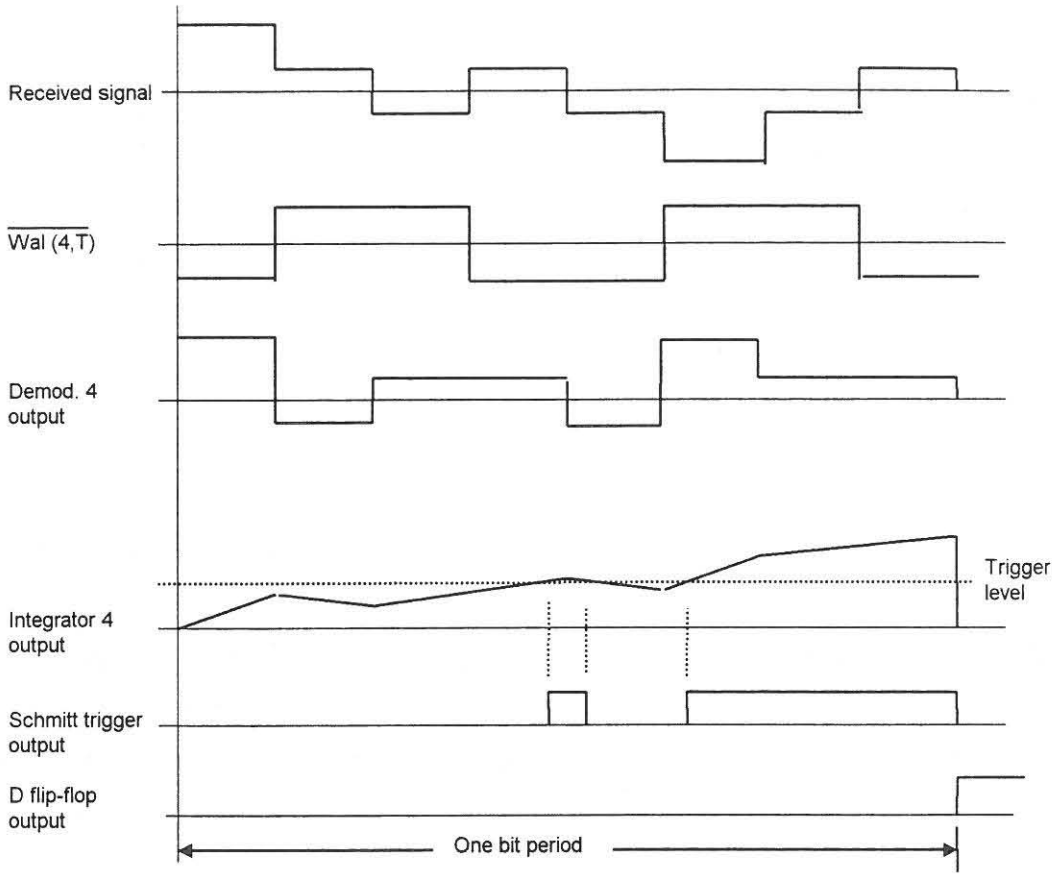


Fig. 4.21 *Typical waveforms in the data recovery filter*

4.1.9.1 Integrator

The circuit diagram of the integrators which have been used is given in Fig. 4.22. [12, pp. 245-260].

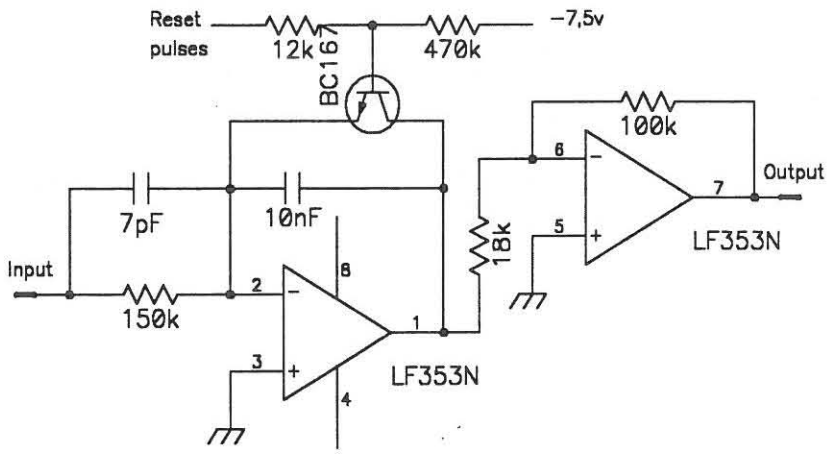


Fig. 4.22 *Integrator circuit diagram*

A 12K resistor is connected in series with the base of each transistor in order that an excessive load will not be placed on the reset pulse source. A negative bias on the base of the reset transistor ensures that it is fully off during the integration period and hence the leakage paths are minimized. The integrator capacitor discharges by a noticeable amount when this bias is removed. The time constant of the R-C network is given by

$$T = 150 \times 10^{3} \times 10 \times 10^{-9} = \underline{1\ 500\ \mu S}.$$

This is somewhat larger than the data interval of 833,3 μS required for a signalling speed of 1 200 bits per second in each channel and good results were obtained using this combination of resistance and capacitance.

A buffer amplifier at the integrator output serves the purpose of isolating the Schmitt trigger from the integrator, and corrects the inversion of polarity that occurs in the integrator. The gain of the buffer amplifiers was set at 6,67 to provide sufficient drive for the Schmitt triggers.

4.1.9.2 Data output circuit

The output from each integrator is taken directly to a Schmitt trigger. A 7414 TTL Hex Schmitt integrated circuit is used for this purpose, and the circuit arrangement is given in Fig. 4.23.

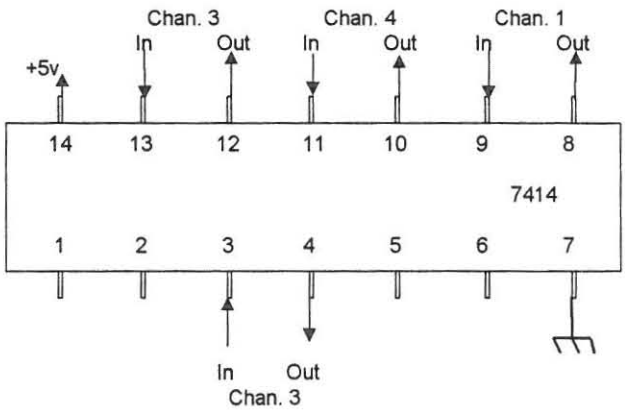


Fig. 4.23 *Schmitt trigger*

The 7414 Schmitt triggers display a large amount of hysteresis which is fortunately not important in this application. These Schmitt triggers turn on at about 1,8 volt and off at approximately 0,9 volt.

The Schmitt trigger may be turned on and off a number of times during an integration period of one data bit as shown in Fig. 4.21. However, the only significant part of the integrated waveform is it's value at the moment the reset pulse occurs. It is at this point that the decision is made as to whether a "1" or a "0" is present.

The Schmitt trigger produces an inverted output and this signal is fed to a D flip-flop which, depending upon the input signal, changes state when a clock pulse is present. Dual 7474 TTL D flip-flops are used to provide the data output from the demultiplexer. The D flip-flop arrangement for channels 1 and 3 is shown in Fig. 4.24. A similar arrangement is used for channels 2 and 4.

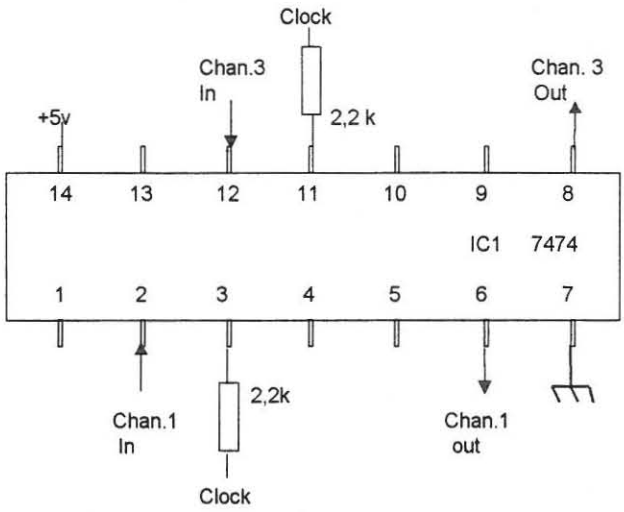


Fig. 4.24 *D Type Flip-flop output circuit*

4.1.9.3 Reset circuit

Input data to the system is made synchronous with *Wal*(1,*t*) as shown by the waveforms in Fig. 4.25.

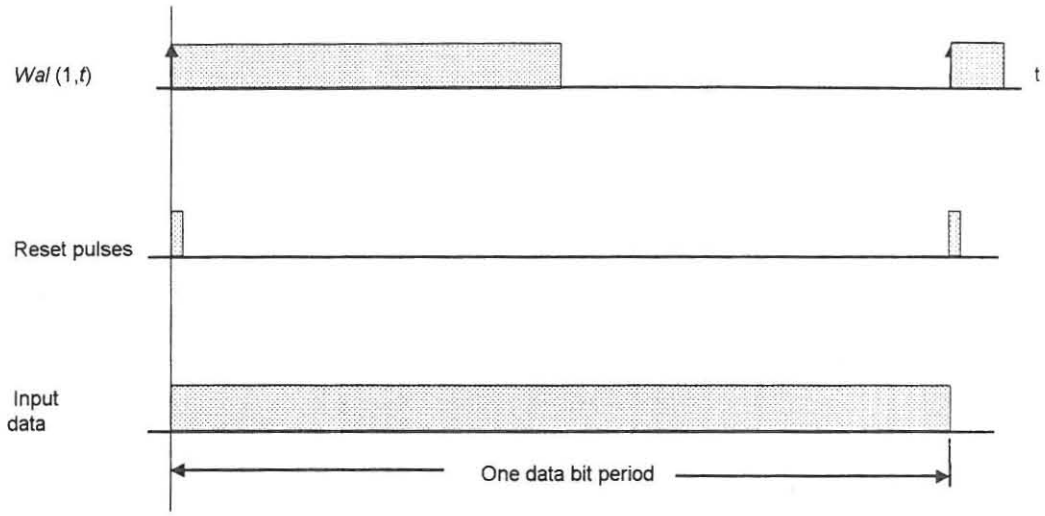


Fig. 4.25 *Timing of Walsh functions, data and reset pulses*

Short reset pulses are required at the end of each data bit for the integrating circuits and for triggering the D flip-flops. These pulses are generated in a 74121 TTL monostable multivibrator integrated circuit. The circuit is triggered by the Walsh function generator and uses the rising edge of *Wal*(1,*t*) for this purpose. The circuit used for generating reset pulses is given in Fig. 4.26.

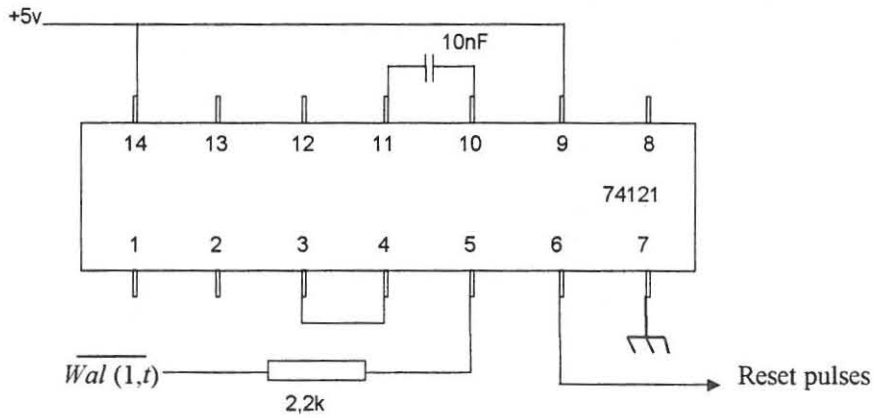


Fig. 4.26 *Reset pulse generator*

The 74121 has an internal resistor of 2K in the monostable circuit. This internal resistor can be used by connecting pin 9 to the +5 V supply. A 10 nF capacitor provides reset output pulses of 14 µS duration.

4.2 DESCRIPTION OF THE BINARY SDM SYSTEM

A binary sequency division multiplexing system consisting of the necessary transmitting and receiving equipment was designed and constructed. Provision was made for four data channels.

The transmitter and receiver were linked by a short piece of cable. As with the multi-level system, the link can readily be opened to insert test equipment in the transmission path.

The clock pulse generator, Walsh function generator and amplifier system of the multi-level system were used to provide the Walsh carriers for the multiplexer and demultiplexer.

As before, power was obtained from analog and digital training equipment.

4.2.1 BLOCK DIAGRAM OF THE BINARY SDM SYSTEM

A simplified block diagram layout of the four channel binary system of sequency division multiplexing is given in Fig. 4.27.

Data is applied to the modulators in each channel together with the relevant Walsh functions. The data inputs are also used to set the level of a slicing circuit for each data bit period.. Since the logic required for this purpose is rather complex a programmable array logic circuit (PAL) has been used to perform the necessary logic operations.

The outputs of the modulators are combined in the summing amplifier and then passed to the adaptive slicer. The slicer output is transmitted as a binary signal.

At the receiver the binary signal is demodulated by the appropriate Walsh function in each channel. The demodulator outputs are passed on to a data recovery filter (DRF) which functions in exactly the same manner as that in the multi-level system.

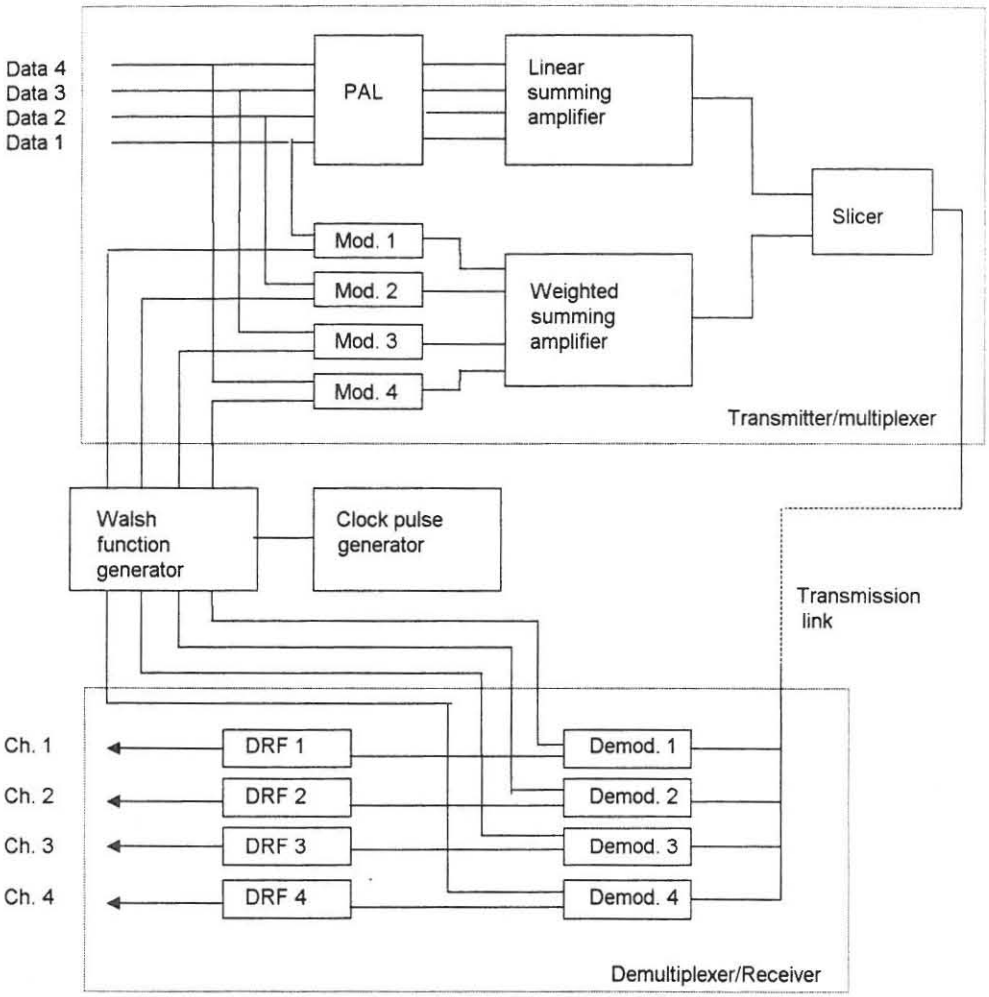


Fig. 4.27 *Basic layout of four-channel binary SDM system.*

4.2.1.1 Walsh function carriers

Walsh functions with only two logic levels, viz 0 and +1 are used for the binary system of DSM. The carrier levels are now re-defined as follows:

Multi-level DSM	*Binary DSM*
+1	0
-1	+1

The system still functions synchronously with the Walsh carriers, but is locked to the falling edge of *Wal* (1,*t*) halfway through it's period.

By locking the Walsh carriers to the falling edge of *Wal*(1,*t*) the phase relationships of *Wal*(3,*t*) and *Wal*(4,*t*) are not strictly correct as compared with *Wal*(1,*t*) and *Wal*(2,*t*). This can be seen by sketching the Walsh functions beyond the period of *Wal*(1,*t*) as in Fig. 4.28.

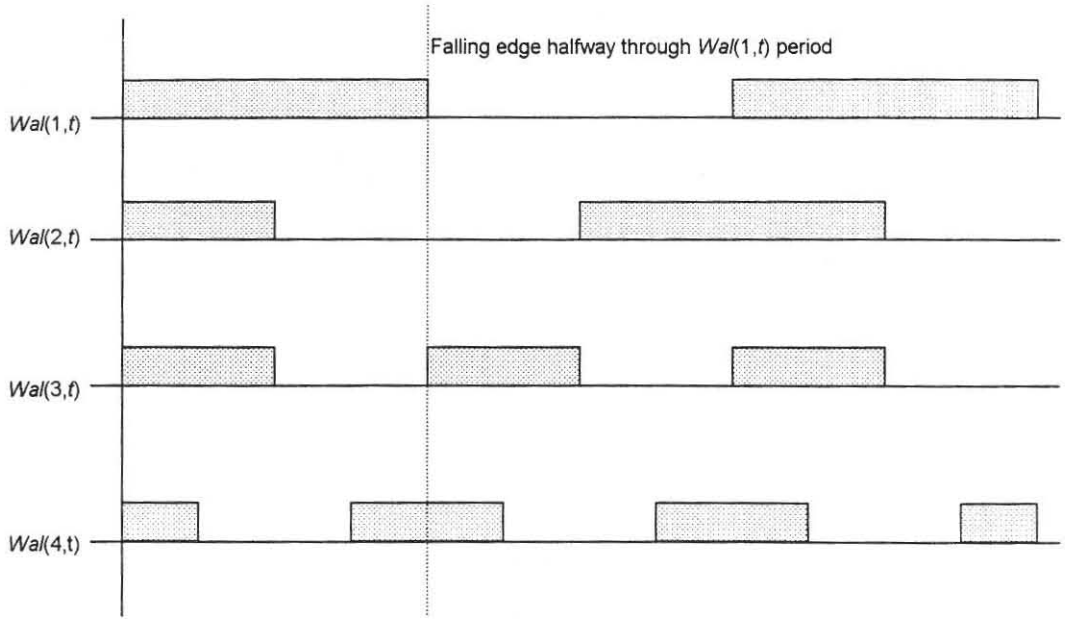


Fig. 4.28 *Phase relations of Walsh functions relative to falling edge of Wal(1,t)*

The broken line indicates the beginning of each Walsh function in the binary system. In order to maintain correct phase relations with *Wal*(3,*t*) and *Wal*(4,*t*) these two carriers are phase inverted by two NOR gates in a 7402 integrated circuit.

4.2.2 MODULATORS

Modulation of the Walsh functions by the input data is performed by exclusive "OR" gates [8, p. 419]. A 7486 TTL quad exclusive OR integrated circuit is used for this purpose. The circuit arrangement is given in Fig. 4.29.

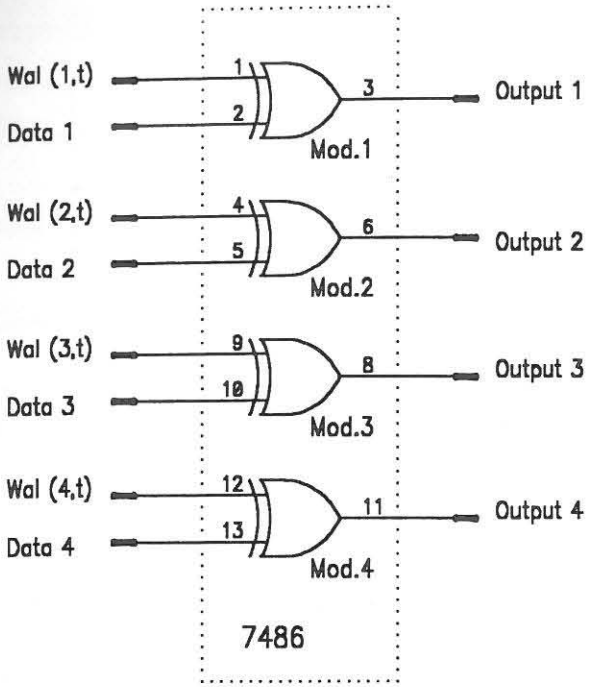


Fig. 4.29 *Exclusive "OR" modulator circuits*

Since 5 volt TTL circuitry is used to perform the function of modulation, the Walsh carrier waveforms must switch between 0 volt and 5,0 volt. The Walsh functions *Wal*(1,*t*), *Wal* (2,*t*), *Wal*(3,*t*) and *Wal*(4,*t*) are used as carriers and are applied to the exclusive "OR" gate inputs at pins 1, 4, 9 and 12 respectively.

Data input signals that switch between 0 volt and +5 volt are connected to the inputs of the four channels at pins 2, 5, 10 and 13.

The modulator outputs are available at pins 3, 6, 8 and 11of the integrated circuit.

The modulator outputs switch between 0 volt and 4,4 volt. The waveforms of the Walsh carriers for one bit period are given in Fig. 4.30.

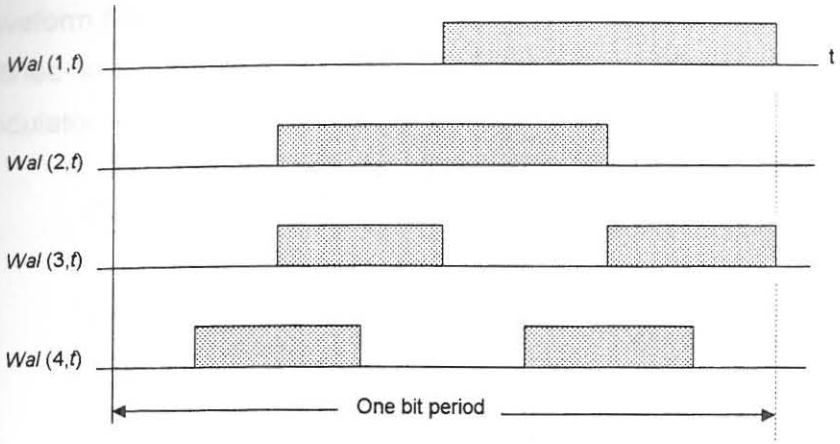


Fig. 4.30 *Set of Walsh functions used with exclusive "OR" modulators*

4.2.2.1 Summing amplifier

The outputs of the four modulators are combined in a 741 operational amplifier summing circuit as shown in Fig. 4.31.

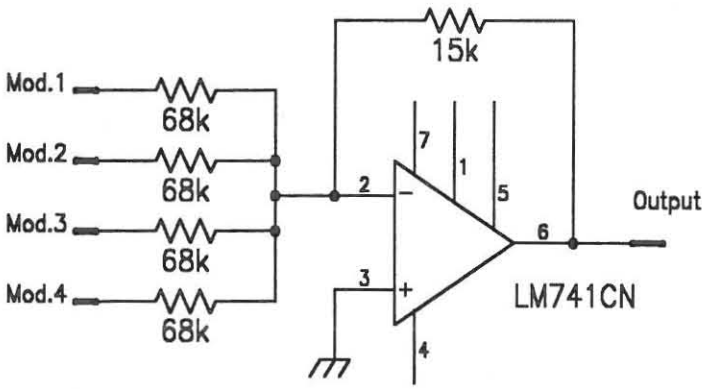


Fig. 4.31 *Linear summing amplifier*

The gain of each channel is determined by the resistor values chosen for the circuit. For the amplifier in Fig. 4.31, the magnitude of the gain is, A_V = 0,220 6.

This value of gain was convenient to obtain an output signal with a maximum value that is roughly the same as the maximum input from each modulator.

When different data inputs are applied to the modulators, the shape of the output waveform from the summing amplifier will change. However, there are four clearly defined levels in the modulator output signal as indicated in Fig. 4.32. The modulator output for a data input of 0010 is given in Fig. 4.32.

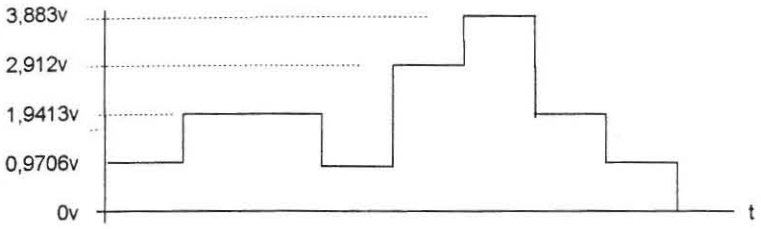


Fig. 4.32 *Summing amplifier output for data inputs of* 0010.

Since the magnitude of the signals from each modulator is 4,4 volt, the size of each of the steps can be calculated as follows:

(a) When all modulator outputs are 0, the output from the summing circuit will also be 0.

(b) When only one modulator output is at 4,4 volt,

$e_0 = 0{,}220\ 6 \times 4{,}4$

$\therefore \quad e_0 = 0{,}970\ 6$ volt (Level 1)

(c) When two modulator outputs are at 4,4 volt each

$e_0 = 0{,}220\ 6 \times (4{,}4 + 4{,}4)$

$\therefore \quad e_0 = 1{,}941\ 3$ volt (Level 2)

(d) When three modulator outputs are at 4,4 volts each

$e_0 = 0{,}220\ 6\ (4{,}4 + 4{,}4 + 4{,}4)$

$\therefore \quad e_0 = 2{,}912$ volt (Level 3)

(e) When four modulator outputs are at 4,4 volts each

$e_0 = 0{,}220\ 6\ (4{,}4 + 4{,}4 + 4{,}4 + 4{,}4)$

$\therefore \quad e_0 = 3{,}883$ volt (Level 4)

These levels are identified in Fig. 4.32

4.2.3 ADAPTIVE SLICER

The output from the modulator summing circuit is sliced in a comparator circuit by comparing it with a level which is set by the specific combination of data inputs. Each of the four steps shown in Fig. 4.33 could be sliced at the levels shown as *w*, *x*, *y* or *z*.

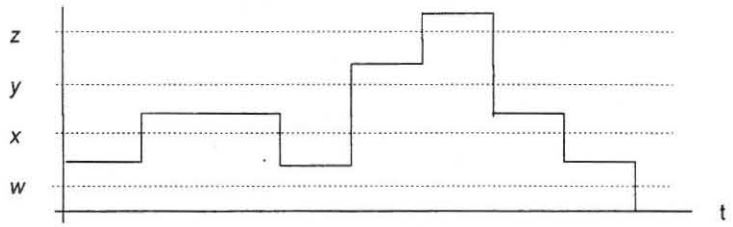


Fig. 4.33 *Slicing levels of modulator output signal*

By inspection of the waveforms for all data input combinations, it was found that the output of the linear summing circuit should be sliced at the levels given in Table 4.3.

Table 4.3 *Slicing levels for all data input combinations*

a	b	c	d	Slice level
0	0	0	0	w
0	0	0	1	w
0	0	1	0	x
0	0	1	1	x
0	1	0	0	x
0	1	0	1	x
0	1	1	0	y
0	1	1	1	y
1	0	0	0	x
1	0	0	1	z
1	0	1	0	y
1	0	1	1	y
1	1	0	0	y
1	1	0	1	y
1	1	1	0	z
1	1	1	1	z

The slicing levels associated with the various data inputs can be arranged in a variable entry map as in Fig. 4.34.

ab \ cd	00	01	11	10
00	w	w	x	x
01	x	x	y	y
11	y	y	z	z
10	x	z	y	y

Fig. 4.34 *Variable entry map of slicing levels*

The following Boolean relations can be derived from the variable entry map.

$$w = \bar{a} \cdot \bar{b} \cdot \bar{c} \tag{4.1}$$

$$x = \bar{a} \cdot \bar{b} \cdot c + \bar{a} \cdot b \cdot \bar{c} + a \cdot \bar{b} \cdot \bar{c} \cdot \bar{d} \tag{4.2}$$

$$y = \bar{a} \cdot b \cdot c + a \cdot b \cdot \bar{c} + a \cdot \bar{b} \cdot c \tag{4.3}$$

$$z = a \cdot b \cdot c + a \cdot \bar{b} \cdot \bar{c} \cdot \bar{d} \tag{4.4}$$

From Table 4.3 it is clear that only one of these expressions has a "1" output for any combination of data inputs. Since the combinational logic required to perform these functions requires a large number of gates, a 16R4 programmable array logic (PAL) integrated circuit has been used for this purpose [19, pp. 24-119].

Since the 16R4 PAL is an "active low" device the complements of equations (4.1) to (4.4) must be used such that:

$$\bar{w} = a + b + c \tag{4.5}$$

$$\bar{x} = \bar{a} \cdot \bar{b} \cdot \bar{c} + a \cdot b + b \cdot c + a \cdot c + a \cdot d \tag{4.6}$$

$$\bar{y} = \bar{a} \cdot \bar{b} + \bar{a} \cdot \bar{c} + a \cdot b \cdot c + \bar{b} \cdot \bar{c} \tag{4.7}$$

$$\bar{z} = \bar{a} + b \cdot \bar{c} + \bar{b} \cdot c + \bar{c} \cdot \bar{d} \tag{4.8}$$

4.2.3.1 PAL logic circuit

The information in Table 4.3 and the Boolean relations (4.5), (4.6), (4.7), (4.8) were used to prepare a 16R4 PAL circuit to perform the required logic for controlling the slicer.

The PAL was programmed according to the relations (4.5) to (4.8) above. Data inputs are connected to pins 3, 4, 5, 6 and the PAL outputs are available at pins 12, 13, 18, 19.

The pin connections of the programmed 16R4 PAL are given in Table 4.4.

Table 4.4 *Pin connections of 16R4 PAL*

Pin 1 :CLK
Pin 2 :INPUT = e
Pin 3 :INPUT = *a*
Pin 4 :INPUT = *b*
Pin 5 :INPUT = *c*
Pin 6 :INPUT = *d*
Pin 10 :GND
Pin 11 :!EN
Pin 12 :OUTPUT = $\overline{w}$
Pin 13 :OUTPUT = $\overline{x}$
Pin 18 :OUTPUT = $\overline{y}$
Pin 19 :OUTPUT = $\overline{z}$
Pin 20 :V_{CC}

The outputs of the PAL must be combined in such a way that the slicer is set more or less in the centre of each amplitude level for the various combinations of data inputs.

Output W must set the slicer to the lowest level, output X sets it to the next higher level, output y sets it to third level and output Z sets it to the highest level. The different levels are obtained by weighting the outputs of the PAL in a summing network.

The PAL is connected to the weighted summing network as shown in Fig. 4.35.

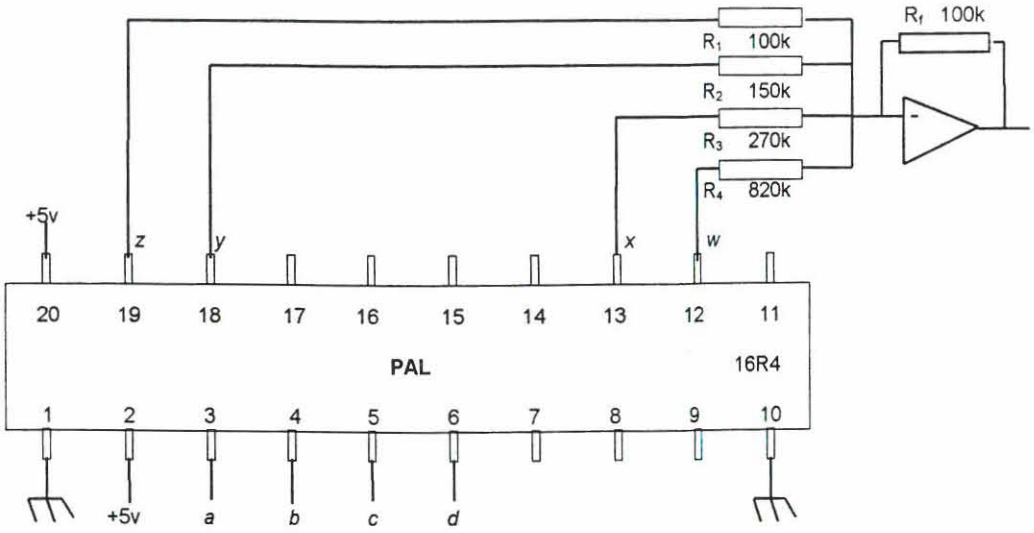


Fig. 4.35 *Connection of PAL in slicer level setting circuit*

When calculating suitable values for the resistors, each of the four steps should be divided into two parts to locate the centre of each riser. These points are shown in Fig. 4.36.

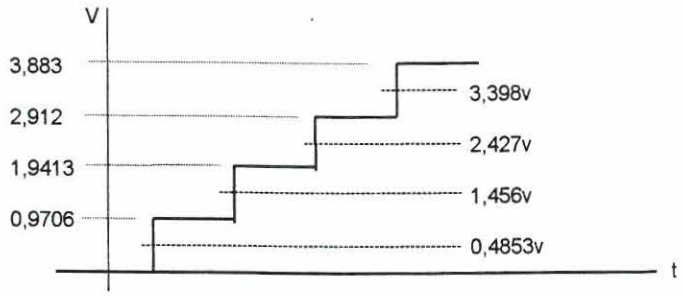


Fig. 4.36 *Location of centre points on steps*

Output voltages from the PAL logic circuits switch between 0 volt and 3,6 volt.

At the centre of the highest step the slicer voltage in Fig. 4.36 is given as 3,398 volt.

Then:

$$V_{slicer} = \frac{R_f}{R_i} \cdot V_{in} \qquad (4.9)$$

The feedback resistor R_f is chosen as 100 kilo-ohm. It was found that when a 5,0 meg-ohm resistor was connected in parallel with the 100 K resistor, the calculated results were closer to standard values of available resistors.

Then, R_f = 98,04 kilo-ohm

Using (4.9) the value of R_1 for the fourth step can be calculated as:

$$3{,}398 = \frac{98{,}04 \times 10^3 \times 3{,}6}{R_1}$$

$$\therefore \quad R_1 = 103{,}9 \text{ k}$$

The nearest standard value of 100 kilo-ohm was used for R_1.

The values of the other resistors are calculated in a similar manner. The nearest standard values were used as indicated below:

	Calculated value	Standard value
R_1	103,9k	100k
R_2	145,4k	150k
R_3	242,4k	270k
R_4	727,3k	820k

The signals at the modulator are fairly stable, with a large signal to noise ratio, and hence the values of these resistors is not critical as long as the slicing level is located at roughly the centre of the step riser.

4.2.3.2 Comparator

During the time interval of each data bit the outputs of the modulation summing circuit is compared with the level set by the PAL logic circuit. The comparator circuit with the linear and weighted summing amplifiers is given in Fig. 4.37.

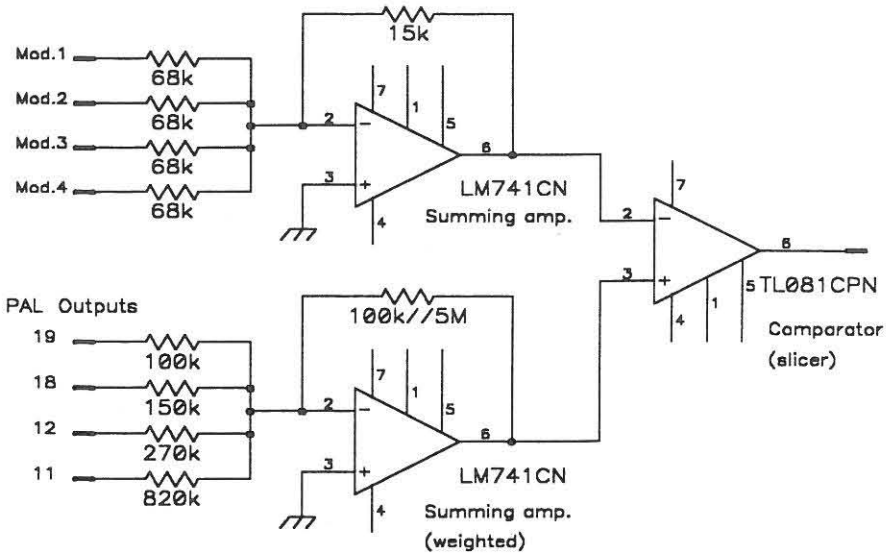


Fig. 4.37 *Comparator Slicer*

A TL081 operational amplifier is used in a standard comparator circuit [6].

The modulator circuit input is connected to the inverting input of the TL081 operational amplifier and the PAL logic circuit to the non-inverting input. The sliced signal is present at the output on pin 6.

The binary slicer comparator output signal is in a suitable form for transmission.

4.2.4 DEMULTIPLEXER

The received binary signals are applied to the inputs of demodulator circuits with the appropriate Walsh functions. The demodulator circuits are exclusive "OR" logic and are similar to the modulators. The circuit arrangement of the demodulators is given in Fig. 4.38. A 7486 quad exclusive "OR" integrated circuit is used for this purpose.

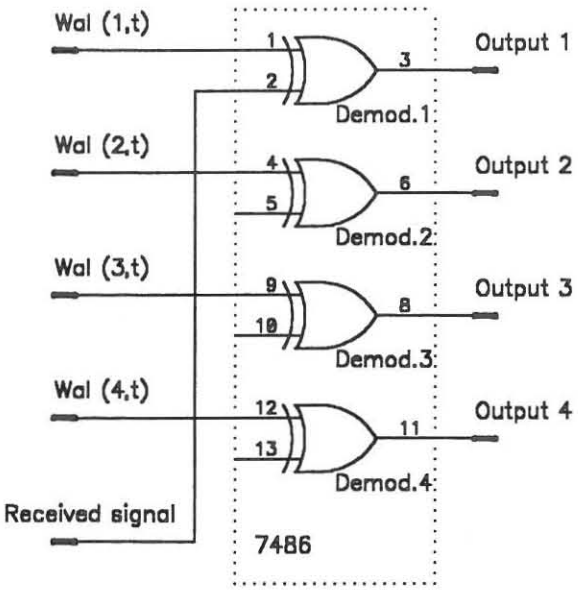


Fig. 4.38 *Demodulator circuit*

The Walsh functions *Wal*(1,*t*), *Wal*(2,*t*), *Wal*(3,*t*) and *Wal*(4,*t*) are connected to pins 1, 4, 9, 12 respectively. The received binary signals are connected to pins 2, 5, 10, 13 as shown. The outputs from each channel are available at pins 3, 6, 8, 11.

4.2.5 DATA RECOVERY FILTER

As with the multi-level sequency multiplex system, the demodulator outputs are passed through a data recovery filter which consists of integrators, Schmitt triggers, and D flip-flops.

The same considerations apply for re-setting the integrators. It is therefore not necessary to discuss this circuit once more.

4.3 SUMMARY

- A clock pulse generator driven by a 6,144 MHz crystal controlled oscillator produces a number of square-wave outputs; viz: 19,8 kHz, 9,6 kHz, 4,8 kHz and 2,4 kHz. One of the outputs is selected to drive a unit pulse generator to

produce a set of block pulse functions. Combinations of the block pulse functions are used to produce the desired set of Walsh functions, viz; *Wal*(1,*t*), *Wal*(2,*t*), *Wal*(3,*t*) and *Wal*(4,*t*).

- The sequency multiplexer consists of four modulator circuits. When the data input modulates a Walsh function, one of three output levels may result viz +5 V, 0 V and -5 V.

- The modulator outputs are summed and produce an octonary multi-level output which is transmitted.

- At the receiver, the octonary signal is multiplied by the Walsh functions in the demodulator circuits. The multiplication is performed in an operational amplifier circuit with a pair of transistors that are turned on and off by the Walsh function in each channel to perform the function of multiplication.

- The data recovery filter uses integrators and Schmitt triggers to recover the original data train of 1's and 0's. The Schmitt trigger output is clocked through a D flip-flop and in the process a 1 bit delay is introduced into the system.

- A reset circuit with a monostable multivibrator is used to clock the D flip-flops, and to reset the integrators.

- The binary system of sequency multiplexing uses four exclusive "OR" gates to perform the function of modulation.

- After summing the modulator outputs, the multi-level signal is sliced at a level which is set by the combination of data-inputs. The sliced binary pulses are transmitted to line.

- At the receiver the process of demodulation is carried out by exclusive "OR" gates.

- The demodulated signals are passed through a data recovery filter to obtain the original data signals.

Chapter 5

SYSTEM EVALUATION

The performance of the multi-level and binary systems of sequency division multiplexing was evaluated by measuring the bit error rate which occurs for different values of signal to noise ratios.

At the transmitter a random data generator was used to provide input test signals for the system. A line simulator consisting of a noise generator, attenuator and filter was used to set the signal to noise ratio and a low-pass filter was employed to limit the frequency band of the transmission link. The line simulator was inserted in the transmission link between the transmitter and receiver. A bit error detector was constructed to measure the bit error rate at the receiver for the different test conditions imposed by the line simulator.

The basic layout of the test set-up is given in Fig. 5.1.

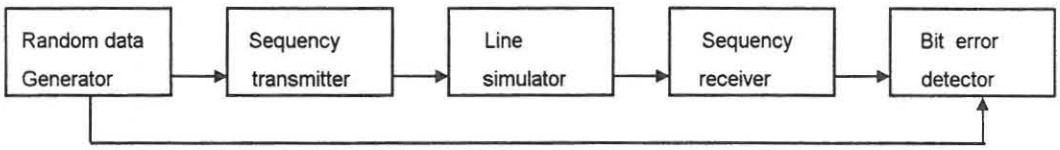


Fig: 5.1 *Block diagram of test set-up.*

Random data bits are applied to the inputs of each of the four channels and these modulate the sequency multiplexer. The modulator outputs are combined and the transmitter output is passed through the line simulator to the receiver. Sequency signals can be degraded in the line simulator by the addition of noise, or frequency band limiting with a low-pass filter.

At the receiver each of the four channel outputs are compared with the input signals at the transmitter in a bit error detector. Differences are recorded by binary counters in each channel.

5.1 RANDOM DATA GENERATOR

5.1.1 BLOCK DIAGRAM

A source of random data signals is required to conduct performance tests on the sequency division multiplexing equipment. Data bits must be synchronous with the set of Walsh functions and provide random data inputs for each of the four channels.

A wide band noise generator was used as the “seed” to provide for the "randomness" of the data generator. Two 16R8 programmable array logic circuits (PAL's) were used in a 16 stage scrambler arrangement as a pseudo-random data generator [4, p. 200].

The basic block diagram layout of the random data generator used is given in Fig 5.2. Note that any of the eight outputs of each PAL may be used.

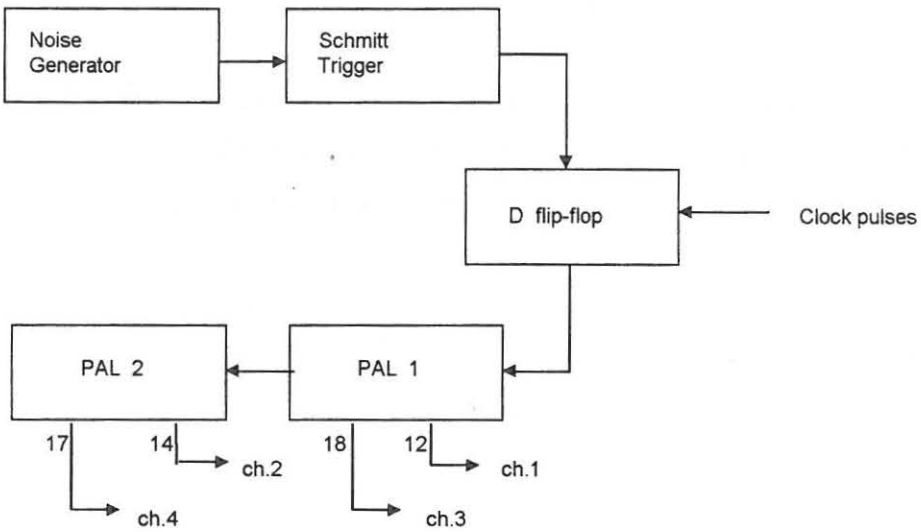


Fig 5.2 *Block diagram of random data generator test set.*

The noise generator output is passed to a Schmitt trigger where noise pulses that are sufficiently large switch the trigger and produce rectangular output pulses of a uniform magnitude. Output pulses from the Schmitt trigger toggle a D flip-flop on a random basis but the data generator acts synchronously with the system clock pulses. Hence, although the state of the D flip-flop cannot be predicted from one clock pulse interval to the next, it's output pulses are synchronous with the system clock. At regular intervals the D flip-flop output is clocked into the PAL pseudo-random data generator circuit. Should a noise pulse

and a clock pulse be present simultaneously, a "l" seed pulse will be clocked into the data generator. The magnitude of the noise generator must be adjusted so that the D flip-flop output produces about equal numbers of 1's and 0's.

The equivalent diagram in Fig. 5.3 may be used to explain the action of the scrambler circuit consisting of the two 16R8 PAL's. Each PAL contains eight flip-flops with an exclusive OR logic gate at the input to each flip-flop [21, pp.568-569].

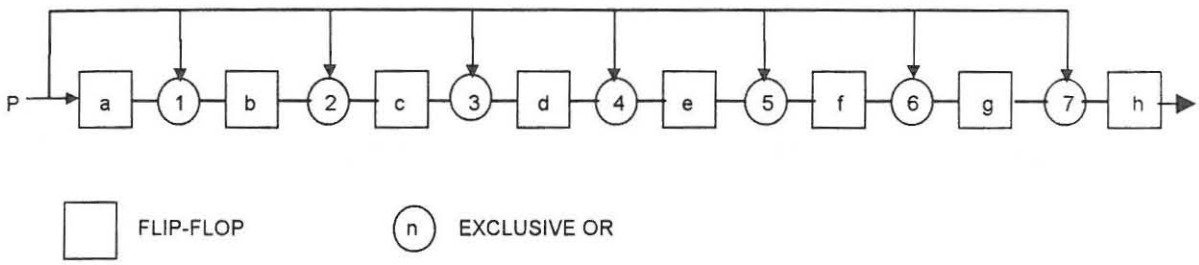


Fig. 5.3 *Equivalent diagram of pseudo-random number generator.*

Assuming that the initial condition of each flip-flop output is 0, and that a constant stream of l's is applied to the input P at the left it is possible to construct Table 5.1. The quantity "n" represents the pulse number at the input to the scrambler.

Table 5.1 *Action of pseudo-random number generator.*

n	P	a	b	c	d	e	f	g	h	
0	1	0	0	0	0	0	0	0	0	
1	1	1	1	1	1	1	1	1	1	
2	1	1	0	0	0	0	0	0	0	
3	1	1	0	1	1	1	1	1	1	
4	1	1	0	1	0	0	0	0	0	
5	1	1	0	1	0	1	1	1	1	
6	1	1	0	1	0	1	0	0	0	
7	1	1	0	1	0	1	0	1	1	
8	1	1	0	1	0	1	0	1	0	Lock up
9	1	1	0	1	0	1	0	1	0	←

The output of flip-flop h is passed on to the input of the next PAL.

If the state of the input does not change before the time a condition known as 'lock-up' will occur after eight clock pulse periods. When lock-up occurs the second PAL will also not toggle any further.

Lock-up also takes place after eight clock periods for a constant stream of 0's at the input. Hence, the 'length' of the circuit is said to be 8. Lock-up will be evident as a repetition of the data code outputs of the generator.

Since a white noise generator is used as a source of input pulses for the data generator the input switches randomly between "I" and "0" and it is most unlikely that lock-up will occur, and even if it does take place the circuit will be reset by the first change in the state of the input pulses.[1]

5.1.2 NOISE GENERATOR

A reverse bias applied to the emitter-base junction of a BC 107 transistor was used as the basis for a wide band noise generator circuit [5, p. 85].

The circuit diagram of the white noise generator is given in Fig. 5.4.

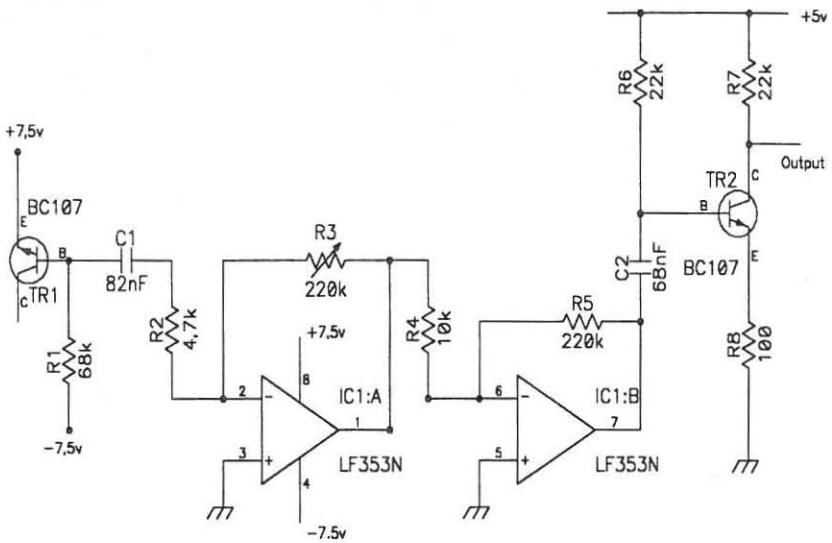


Fig. 5.4 *Noise generator circuit.*

[1] The frequency distribution of the circuit using outputs 12 and 18 on PAL 1 and outputs 14 and 17 on PAL 2 is given in Fig. 5.7

As the +5v supply is too low to produce a satisfactory breakdown in the emitter-base junction of the transistor the +7,5v and -7,5v supplies are used to provide a 15v supply for this purpose. Current flowing through the reverse biased junction produces a white noise spectrum. This noise voltage is too small to switch the Schmitt trigger directly and hence a wide band amplifier circuit was included as shown. The noise generator output was displayed on a personal computer using a fast Fourier transform (fft) to examine the frequency spectrum of the noise produced and the results are given in Fig. 5.5.

Switches are provided at the summing amplifier input to facilitate measurement of the noise level or sequency signal amplitude.

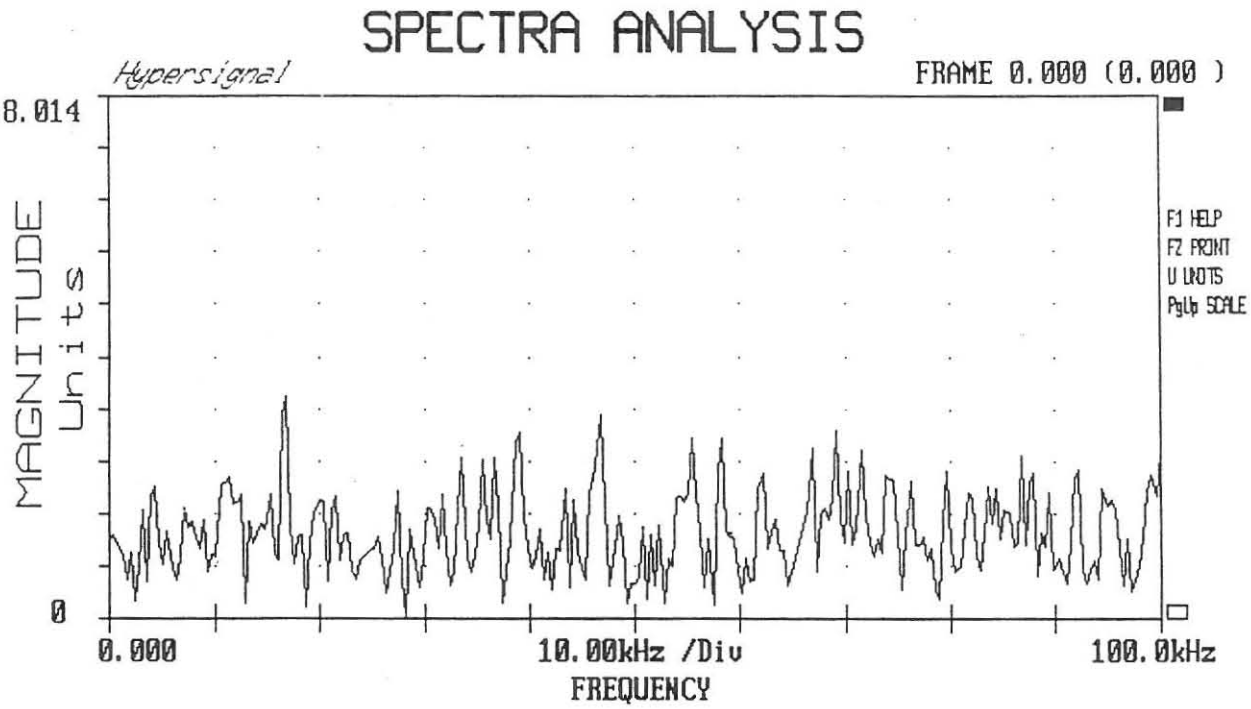


Fig. 5.5 *Noise generator frequency spectrum.*

5.1.3 PSEUDO-RANDOM DATA GENERATOR.

Two 16R8 programmable array logic circuits (PAL's) connected as in Fig. 5.6 are used to produce random data outputs at pin numbers 12, 13, 14, 15, 16, 17, 18, 19. on each PAL.

Pulses from the noise generator are applied to pin 2 of PAL 1 and the output from pin 19 of PAL 1 is used as an input on pin 2 of PAL 2.

The pin connections and Boolean expressions for the 16R8 PAL's are given in Table 5.2.

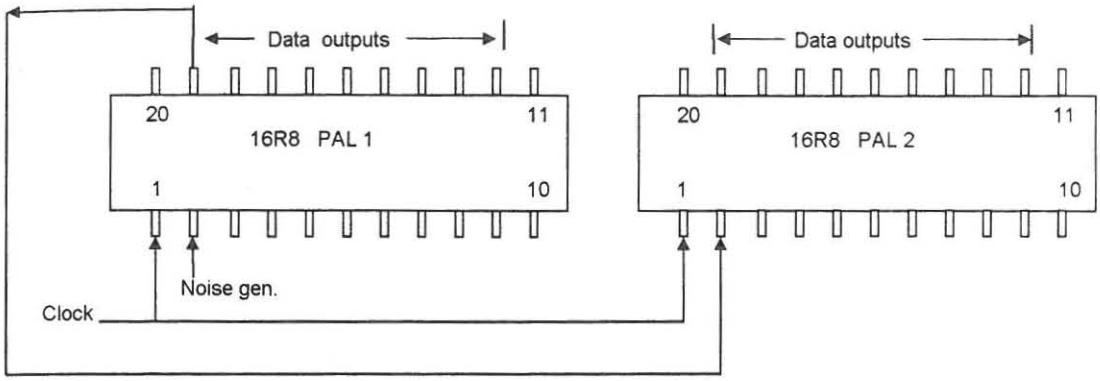


Fig. 5.6 *Random data generator circuit diagram.*

Table 5.2 *Test vectors of 16R8 PAL's*

	PAL 1	PAL 2
Pin 1	Clock	Clock
Pin 2	Input = !P	Input = !h
Pin 3	Input =	Input =
Pin 4	Input =	Input =
Pin 5	Input =	Input =
Pin 6	Input =	Input =
Pin 7	Input =	Input =
Pin 8	Input =	Input =
Pin 9	Input =	Input =
Pin 10	Gnd	Gnd
Pin 11	!EN	!EN
Pin 12	Output = !a	Output = !i
Pin 13	Output = !b	Output = !j
Pin 14	Output = !c	Output = !k
Pin 15	Output = !d	Output = !l
Pin 16	Output = !e	Output = !m
Pin 17	Output = !f	Output = !n
Pin 18	Output = !g	Output = !o
Pin 19	Output = !f	Output = !p
Pin 20	V_{cc}	V_{cc}

Pin 12		
Expression	!a = !p	!l = !ph + p!h
Pin 13		
Expression	!b = !pa + p!a	!j = !pi + p!i
Pin 14		
Expression	!c = !pb + p!b	!k = !pj + p!j
Pin 15		
Expression	!d = !pc + p!c	!l = !pk + p!k
Pin 16		
Expression	!e = !pd + p!d	!m = !pl + p!l
Pin 17		
Expression	!f = !pe + p!e	!n = !pm + p!m
Pin 18		
Expression	!g = !pf + p!f	!o = !pn + p!n
Pin 19		
Expression	!h = !pg + p!g	!p = !po + p!o

The noise generator input is used as a "seed" input at pin 2 of PAL 1 and the output of PAL 1 is used to drive PAL 2.

Data outputs may be taken from pins 12, 13, 14, 15, 16, 17, 18, 19 for the inputs to each channel of the sequency multiplex system.

The output of the random data generator was tested using a Philips PM 3543 logic analyser. Tables 1 to 3 in appendix B gives the results of three test runs with 255 results each. Note that the logic analyser displays the results in hexadecimal form.

Four of the sixteen possible data outputs have been used and the frequency with which each of the hexadecimal quantities 0, 1, 2,.....E, F were recorded is plotted as a histogram in Fig 5.7. The results of test runs 1 to 3 were combined to prepare the histogram. These tests indicate that the output of the data generator is sufficiently random to evaluate the performance of the four-channel sequency division multiplex system.

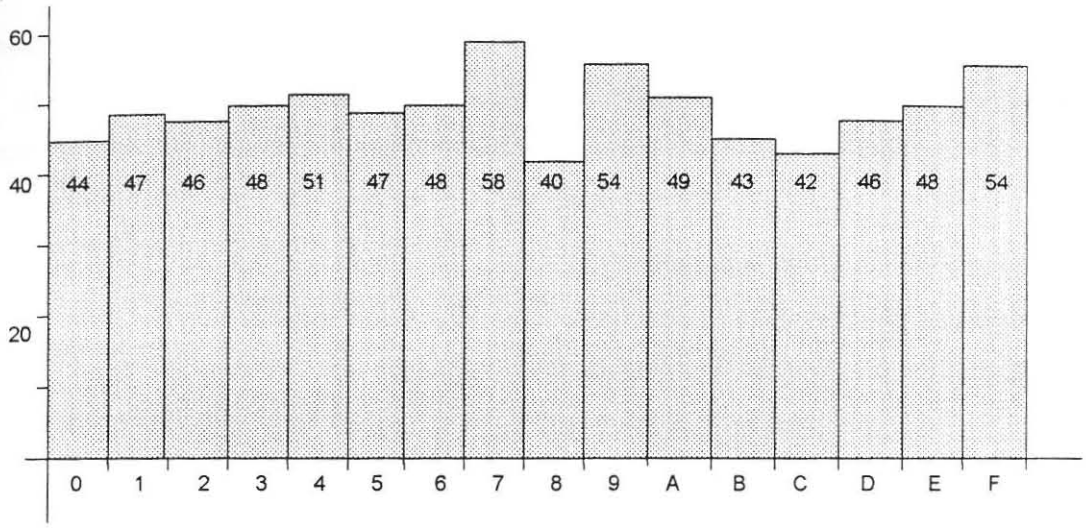


Fig. 5.7 *Frequency of data outputs*

5.2 LINE SIMULATOR

The block diagram layout of the line simulator is given in Fig. 5.8.

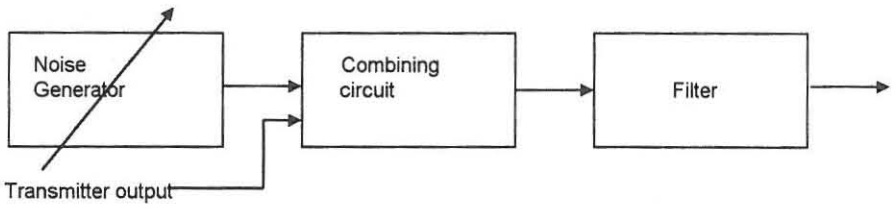


Fig. 5.8 *Block diagram of line simulator.*

The noise generator output is added to the sequency signals in an operational amplifier summing circuit. The output of the noise generator can be adjusted to give the required signal to noise ratio.

A fourth order Butterworth filter in the line simulator is used to limit the harmonic content of the sequency signals and the frequency band of the noise component is also made the same as that of the sequency signals.

5.2.1 NOISE GENERATOR AND UNITY GAIN AMPLIFIER

A similar noise generator to that employed for the pseudo-random data generator was used. Noise is added to the sequency multiplexed signals in a non-inverting unity gain LM 353 operational amplifier circuit. The circuit diagram is given in Fig. 5.9.

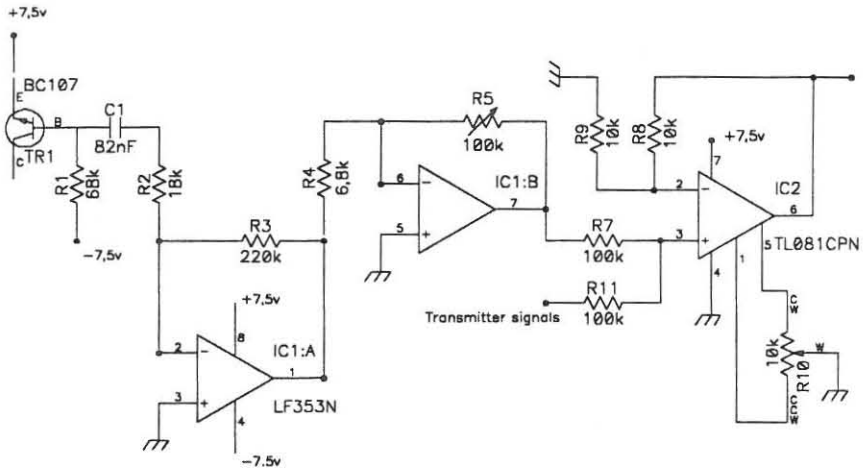


Fig. 5.9 *Noise generator and unity gain amplifier*

Sequency division signals are applied to the input of the unity gain amplifier at R_{11} and noise is introduced at R_7. The magnitude of the noise signals is controlled with R_5.

5.2.2 LOW-PASS FILTER

A fourth order low-pass Butterworth filter was used to determine the effect of limiting the frequency range of the transmission link on the performance of the system.

The circuit arrangement of the filter is given in Fig. 5.10.

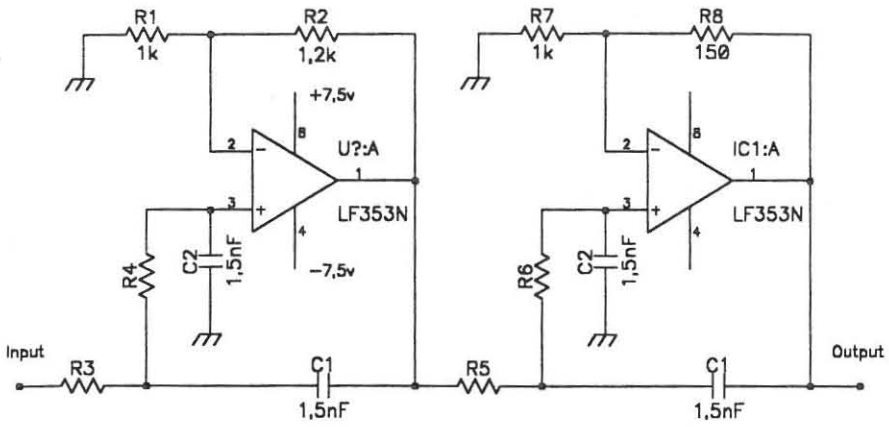


Fig. 5.10 *Fourth order Butterworth filter.*

The following design equations were employed [14, p. 11-27].

$$f_c = \frac{0{,}159}{R.C} \qquad (5.1)$$

$$A_v = 3 - a \qquad (5.2)$$

$$A_v = 1 + R_2 / R_1 \qquad (5.3)$$

For a fourth order filter the term "a" has two values, viz: 0,765 and 1,848.

When a = 0,765, A_v = 2,235.

Suitable values for R_1 and R_2 were taken as: R_1 = 1,0kΩ, and R_2 = 1,2kΩ

When a = 1,848, A_v = 1,152.

In this case suitable values for R_1 and R_2 were found to be: R_1 = 1,0kΩ and R_2 =150Ω.

A convenient value of 1,5nF was chosen for the capacitors C and the value of R was then calculated as 4,7 kΩ, 5,6kΩ and 6,8kΩ for filters with cut-off frequencies of 22,5kHz, 27kHz and 58,9kHz respectively

The frequency response curves of these filters are given in Fig 5.11.

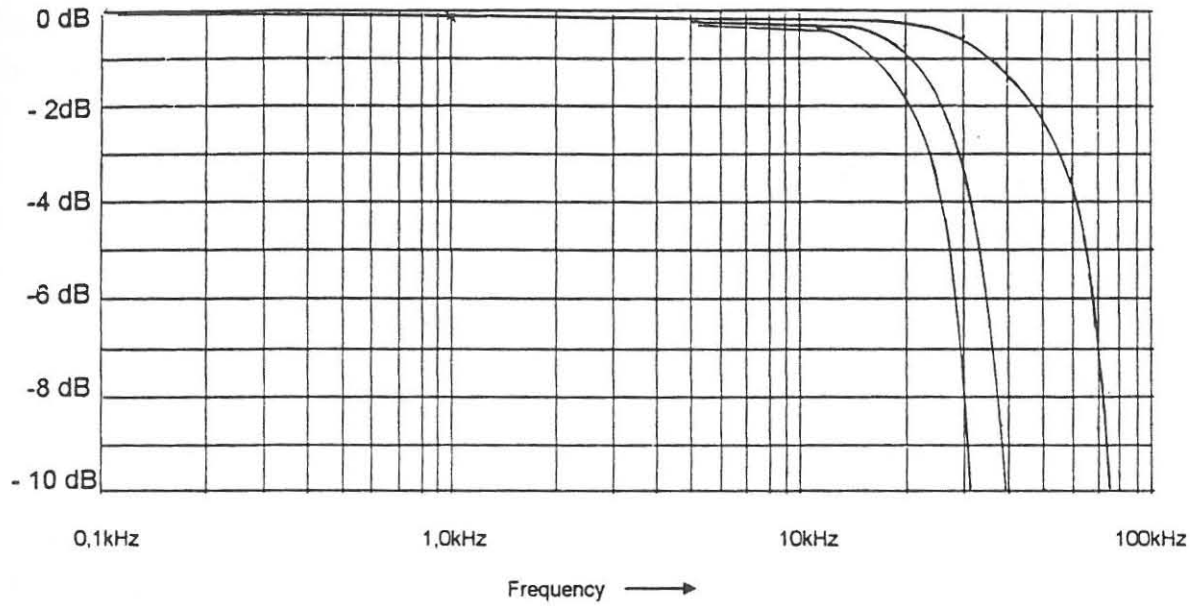


Fig : 5.11 *Frequency response of low-pass filters*

The filter unit was constructed on an Analog Designer board.

An audio oscillator (GW model GAG808B) and an oscilloscope (Kenwood model CS 4025) were used to measure the frequency response of the filters. The response curves were found to approximate the calculated cut-off values very closely.

A Rhode and Schwartz video noise meter BN 120312 was used to measure the rms values of the noise and sequency multiplex signals. The meter was positioned at the filter output in the line simulator. The magnitude of the sequency signals was measured with the noise input switched off. Then the sequency signals were switched off and the noise generator was adjusted to give the required signal to noise ratio. Sequency signals were restored to the input and, after resetting the counters to zero, test runs of 30 minutes duration were conducted.

5.3 BIT ERROR DETECTOR

In order to measure the number of errors that occur in each channel it is necessary to compare the received signals in each channel, bit by bit, with the transmitted signals. The block diagram arrangement of the bit error detector is given in Fig. 5.12.

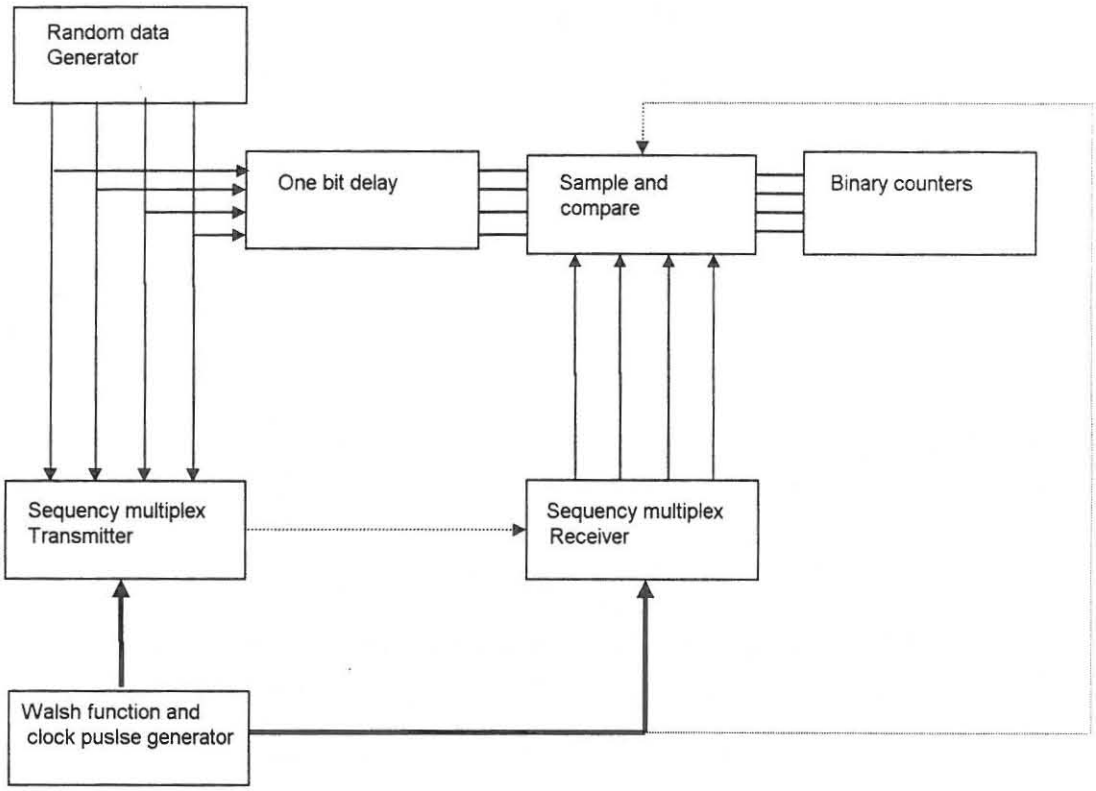


Fig. 5.12 *Block diagram of bit error detector*

Outputs from the random data generator feed the input of each channel, as well as the bit error detector.

Since the data recovery filter in the receiver introduces a one bit delay in the transmission of data it is necessary to provide a corresponding one bit delay in each channel of the bit error detector. This delay is obtained by clocking the data bits through 7474 flip-flop circuits.

Outputs from each of the four channels of the data recovery filter in the sequency receiver are compared with the outputs of the delay circuits in the bit error detector.

Comparison of the pseudo-random data generator output pulses with pulses that have passed through the sequency multiplex system is accomplished in 7486 exclusive OR circuits.

The outputs from each exclusive OR gate is used to drive a binary counter circuit.

Error signals from the four channels are combined in "OR" logic gates to provide a total count as a tally for the counters in each channel.

The circuit diagram of the one bit error detector is given in Fig.5.13.

The total errors output of the 7402 NOR gate was applied to a separate counter (Fluke model 1900A).

The positive edge of Walsh function Wal (1,t) is used to trigger a 74121 monostable with a delay period equal to one data bit. The positive edge of the monostable output is used to clock data through the 7474 bistables.

Outputs from the 7474 bistables are compared with the data outputs from the data recovery filter in the sequency receiver as in Fig. 5.12 The comparison is performed by the 7486 exclusive-OR gates. Outputs from the gates are sampled in the centre of each data bit.

The sample instruction is obtained from a second 74121 monostable circuit. This monostable is also triggered by Wal (1,t), but it has a shorter delay period corresponding to one half the duration of a data bit.

5.3.1. BINARY COUNTER CIRCUIT

The binary counters in each channel employ 7493 ripple through counters with LED displays as in Fig 5.14.

A reset switch is used to set all the bistables to zero before starting a test run.

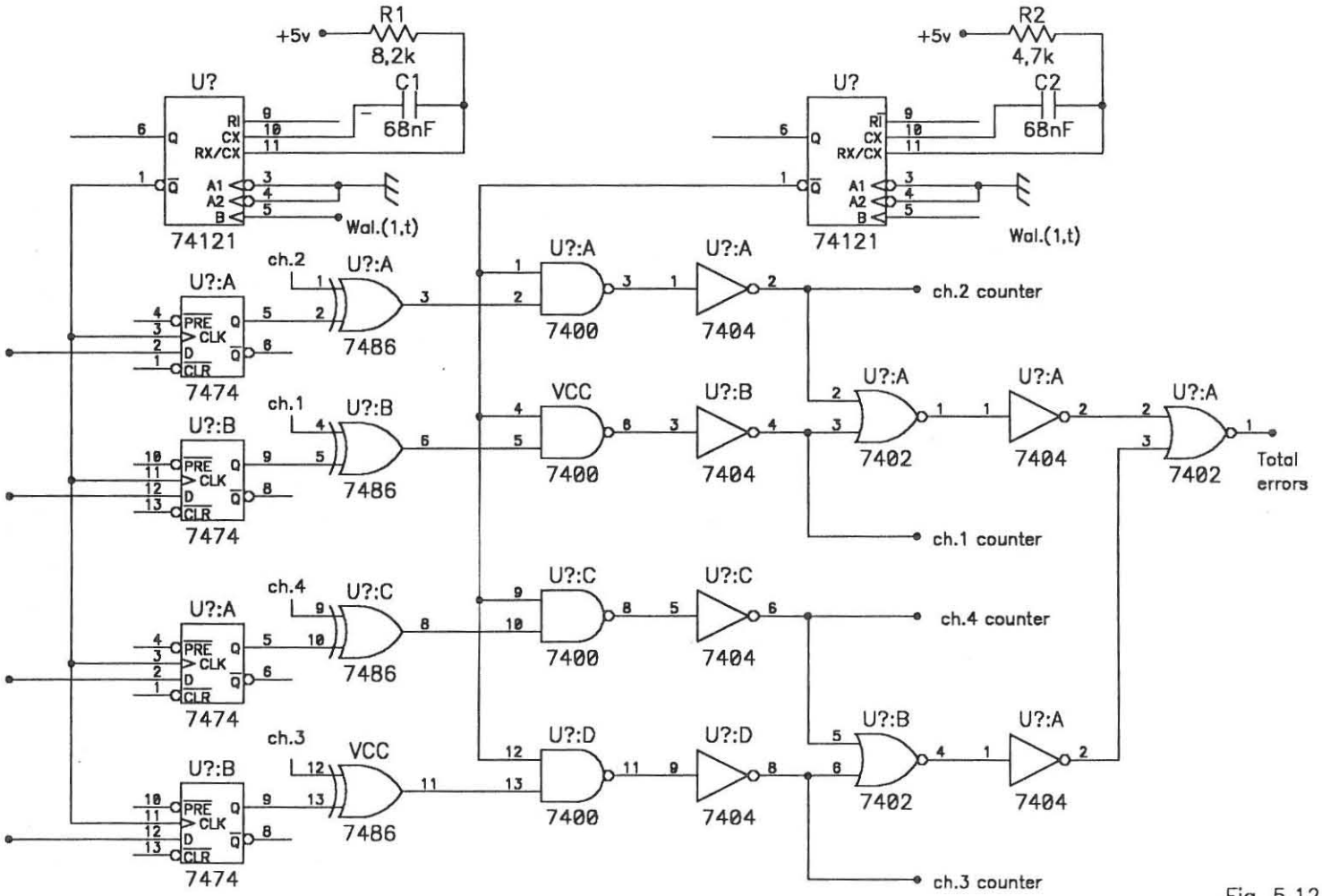


Fig. 5.12

Fig. 5.13 *Circuit diagram of bit error detector*

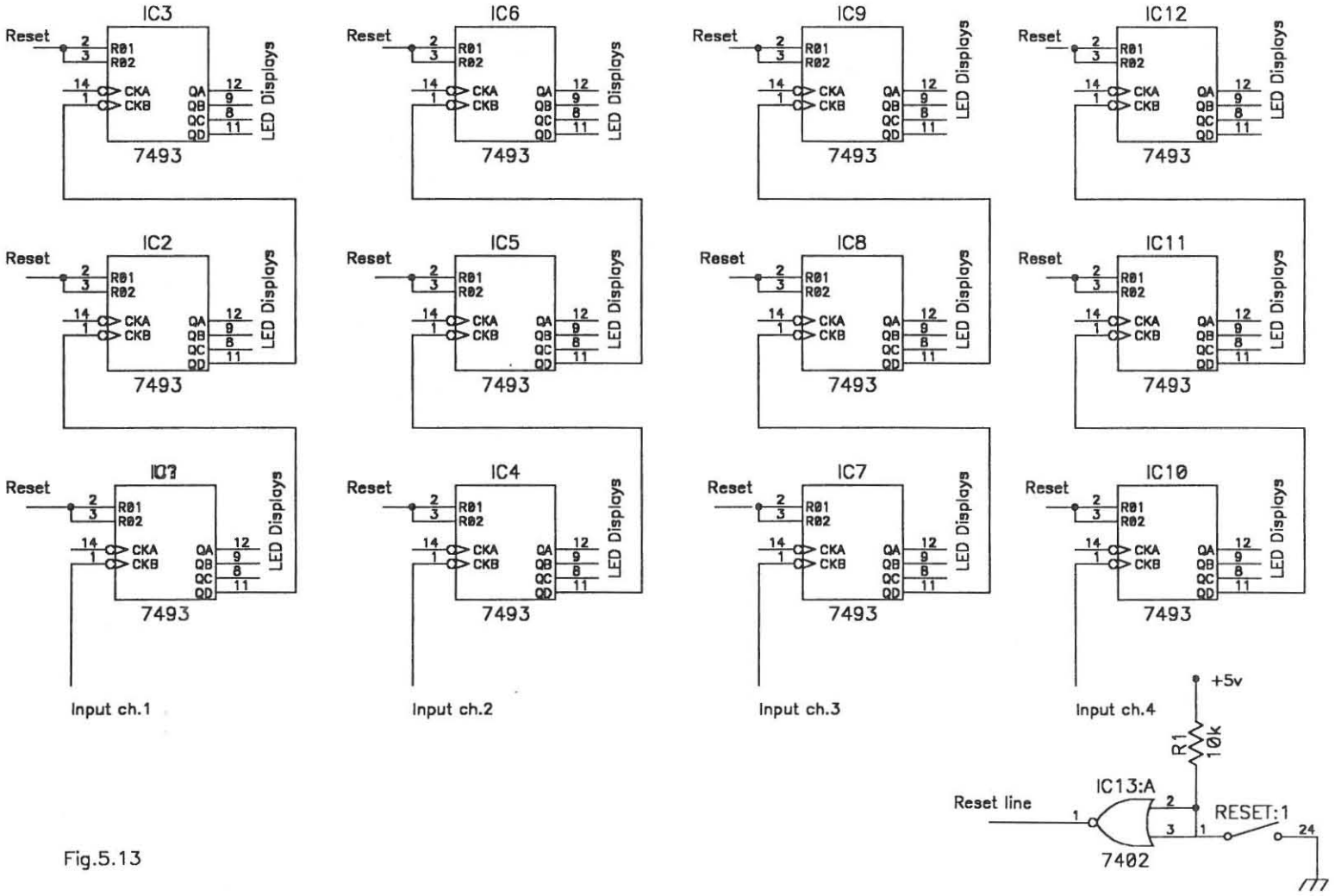


Fig.5.13

Fig. 5.14 *Binary counter circuit diagram*

5.4 FREQUENCY SPECTRA OF SDM SIGNALS

The frequency spectra of sequency division multiplexed signals were examined using a MathCAD computer simulation. (See appendix D)

Since the first four Walsh functions are periodic they were generated directly from sine waves.

Data rates of 1/2, 1/3 and 1/4 of the first Walsh function Wal(1,t) were used to modulate the Walsh carrier, Wal(1,t), and the fast Fourier transform (fft) function was employed to display the resulting frequency spectra.

In each case the modulated signal displayed a strong lower sideband component and an upper sideband with an amplitude that is about 6dB less than that of the lower sideband.

As expected for square wave signals, a series of odd harmonic components were also present.

The binary system of SDM was simulated by a set of Walsh carriers that switch between 1 and 0. When modulated by a "1" in an exclusive OR circuit the Walsh function is effectively inverted. The same result was obtained simply by replacing the > in the appropriate carrier equation by <.

The Walsh carriers Wal(1,t) and Wal 3,t) were modulated logic 1 and the resulting four carriers were summed to form a multi-level signal which was then sliced at an amplitude of 3.7 resulting in a binary signal. The frequency spectrum of this binary signal shows that it is rich in harmonics and hence one may expect that such a binary system would necessitate the use of a larger frequency band.

Measurements of typical SDM signals were taken on the multi-level and binary systems using a personal computer with a PC30 card. Waveforms in the time domain and frequency spectra of the signals are given in appendix E.

The waveform of a modulated Walsh carrier Wal(1,t) is given in Fig. E 1, and it's frequency spectrum in Fig. E 2. The upper and lower sidebands can be seen close to the fundamental frequency line of the carrier.

A typical multi-level SDM signal is shown in Fig. E 3 while it's frequency spectrum is given in Fig. E 4. Two fundamental frequency lines are visible in this figure. These represent Wal(1,t) and Wal(3,t). Note that the frequency of Wal(3,t) is twice that of Wal(1,t).

Fig. E 5 shows the waveform of a typical binary SDM signal and it's frequency spectrum is given in Fig. E 6. The amplitude of the harmonics suggest that the binary system may require a larger frequency band than the Multi-level system.

5.5 SUMMARY

- A pseudo random noise generator was constructed to provide random test data for each of the four sequency multiplex channels.
- A white noise generator was constructed to facilitate performance measurements on the sequency division multiplex systems.
- Fourth order Butterworth filters were used to limit the frequency band of the transmission link.
- An error detector was constructed to count the number of errors that occur in each channel over a given period of time.
- Frequency spectra of the SDM signals were examined using a MathCAD simulation and fast Fourier transforms.

Chapter 6

EVALUATION RESULTS

6.1 INTRODUCTION

Results obtained from measurements taken on the four-channel multi-level and binary systems of sequency division multiplexing are presented in this chapter.

Each system was tested, first of all, using static testing by applying all the binary codes, 0000....1111, manually in turn to the inputs of the four channels using switches and noting that these codes were correctly reproduced by the receiver.

After this dynamic tests were conducted on the two systems using the random data generator to provide input data at a rate of 1 200 bits per second for each of the four channels.

Noise was then introduced into the transmission path at the line simulator. The systems were tested at different signal to noise ratios when low pass filters of 58,9kHz, 27kHz and 22,5kHz were placed in turn in the transmission path. The results of these tests are tabulated in Appendix C in tables C.1 to C.6. Results of tests on the multi-level system are given in tables C.1 to C.3, and for the binary system in tables C.4 to C.6.

Bit error rate tests for different levels of signal-to-noise ratio were conducted on both the multi-level and binary systems of sequency division multiplexing using the test equipment discussed in chapter 5 with the arrangement given by the block diagram in Fig. 5.1.

The tests were conducted for all channels in use. The effects on the BER of using fewer of the available channels has not been investigated in this study.

Low pass filters of 22,5kHz, 27kHz and 58,9kHz were used in the line simulator to assess the performance of the two systems when the sequency signals are band limited.

With random data applied to the system input at a rate of 1 200 bits per second in each channel, and the noise generator output set to zero the rms magnitude of the transmitted multi-channel signal was measured at the output of the line simulator.

With the sequency signals switched off the noise generator output was increased to give the required signal to noise ratio. The sequency signal was switched on again and the rms value of the signal with noise noted.

The binary channel counters, and the total error counter, were set to zero before starting each test run.

Test runs of 30 minutes each were taken for every set of conditions. The number of bits, N, passing through each channel during an interval of 30 minutes was calculated as:

$$N = 1\,200 \times 30 \times 60$$

$$\therefore \quad N = 2{,}16 \times 10^{6} \text{ Bits per second}$$

The number of errors in each channel, Ec, were recorded, as well as the total number of errors, Et, that occurred. As errors sometimes occur simultaneously in two or more channels the total count may sometimes be slightly less than the arithmetic sum of the errors in each of the four channels.

The bit error rate in each channel was calculated as:

$$\text{Channel BER} = Ec/2{,}16 \times 10^{6}$$

The total, or overall, bit error rate for the four channels was calculated as:

$$\text{Total BER} = Et/8{,}64 \times 10^{6}$$

Error rates were measured on both systems for different values of signal to noise ratio using each of the low pass filters in turn.

6.2 DISCUSSION OF TEST RESULTS FOR THE MULTI-LEVEL SYSTEM

The results of the bit error rate tests on the multi-level system are given in tables C.1 to C.3 in appendix C.

The overall (total) bit error rate that was measured when the 22,5kHz, 27kHz and 58,9kHz low-pass filters were used in the line simulator is illustrated by the graphs in Fig.6.1.

These graphs show that there is a significant degradation of noise immunity when the frequency band is limited. This is evident by the spacing between the lines for the 58,9kHz and 22,5kHz filters. For example, at a signal to noise ratio of 7,0dB the BER worsens from about 10^{-6} to about 10^{-3} when the upper frequency limit is reduced from 58,9kHz to 27kHz.

This degradation of noise immunity is to be expected as the filters introduce severe waveform distortion by suppressing harmonics and produce phase distortion as well. This will impair orthogonality of the signals in the four channels and results in cross talk between them leading to errors in the outputs of the four channels at the receiver [2, p. 233].

Bit error rates that were measured in each channel when the low-pass filters of 22,5kHz, 27kHz and 58,9kHz were inserted in the line simulator are given by the curves in Fig. 6.2, Fig.6.3 and Fig.6.4 respectively.

Inspection of the lines in Fig. 6.2 to Fig. 6.4 shows that the differences between the channels become more marked as the cut-off frequency is reduced. While only small differences between the channels are evident in Fig.6.4 for a cut-off frequency of 58,9kHz, considerable differences between the channels are indicated by the curves in Fig.6.2 for a filter cut-off frequency of 22,5kHz.

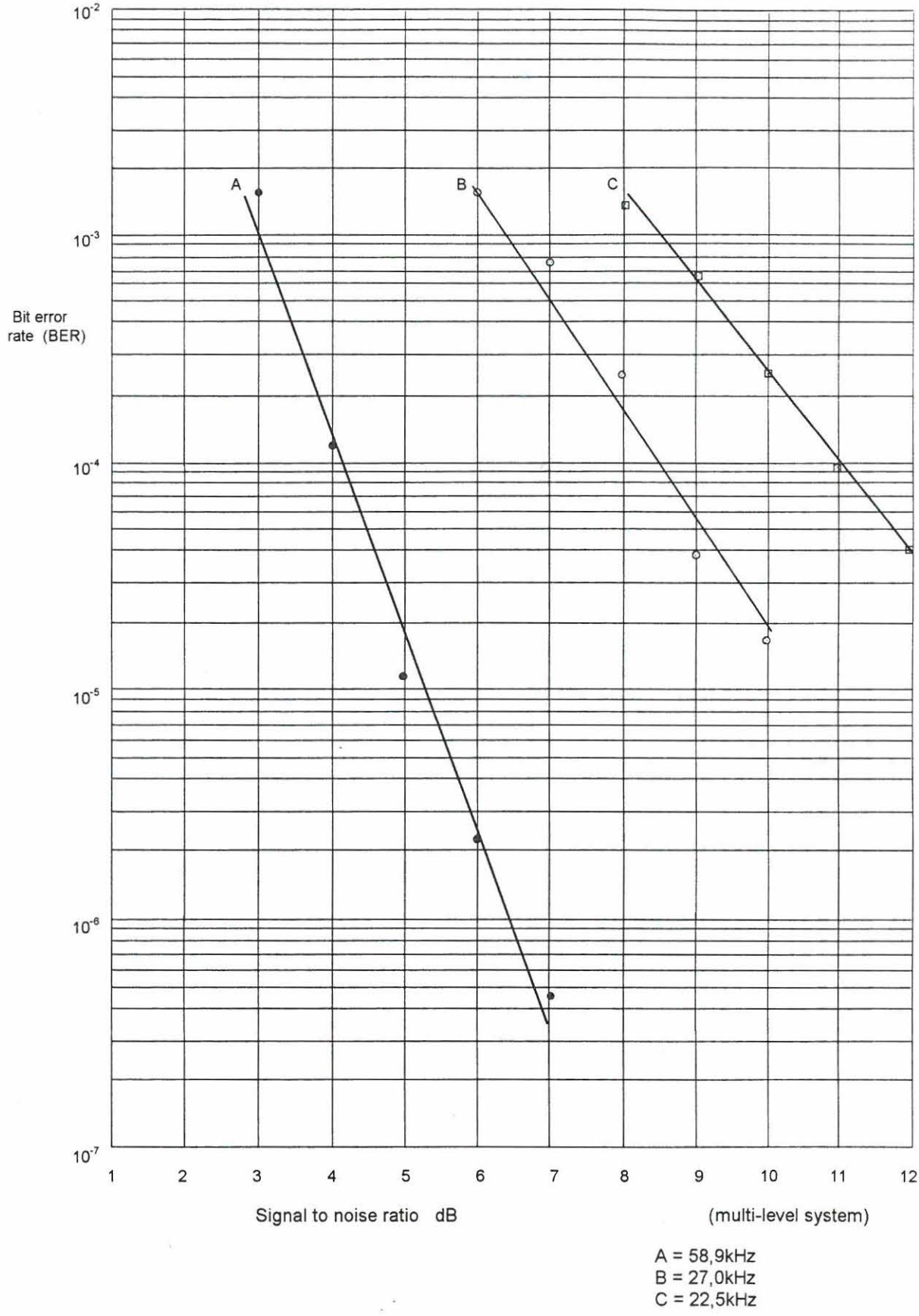


Fig. 6.1 *Overall BER for cut-off frequencies of 22,5kHz, 27kHz and 58,9kHz*

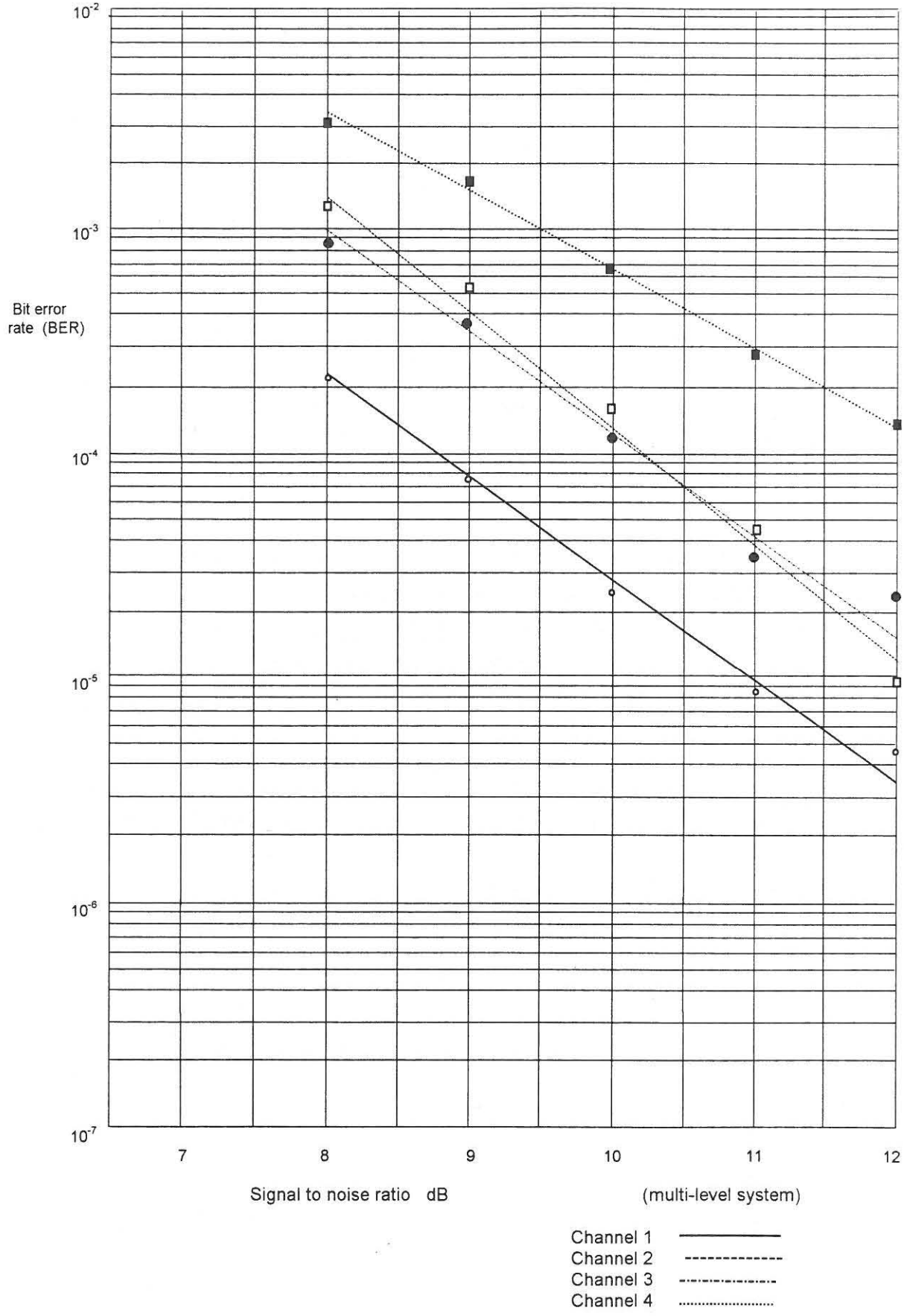


Fig. 6.2 *BER in each channel for a cut-off frequency of 22,5kHz*

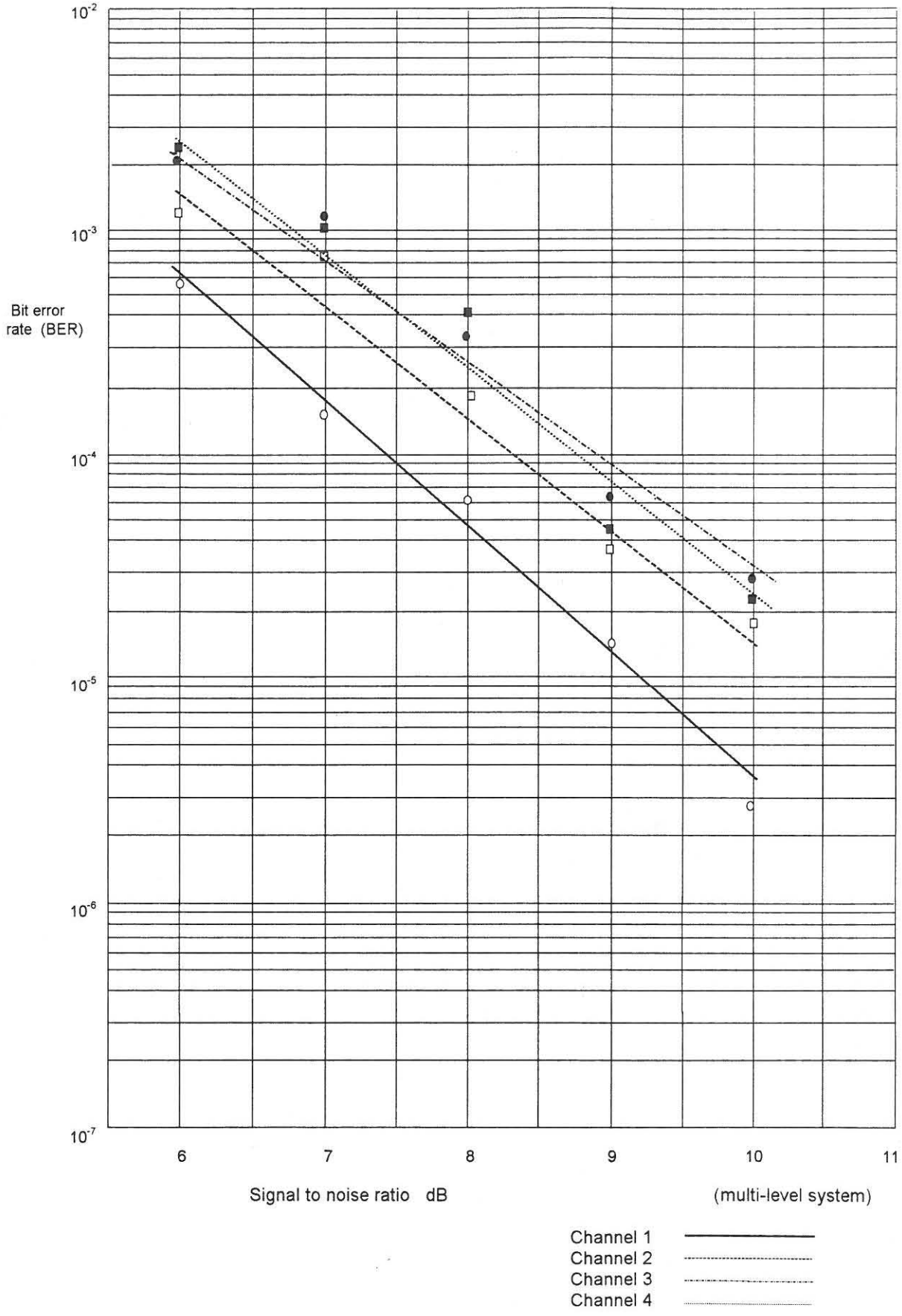


Fig. 6.3 *BER in each channel for a cut-off frequency of 27kHz*

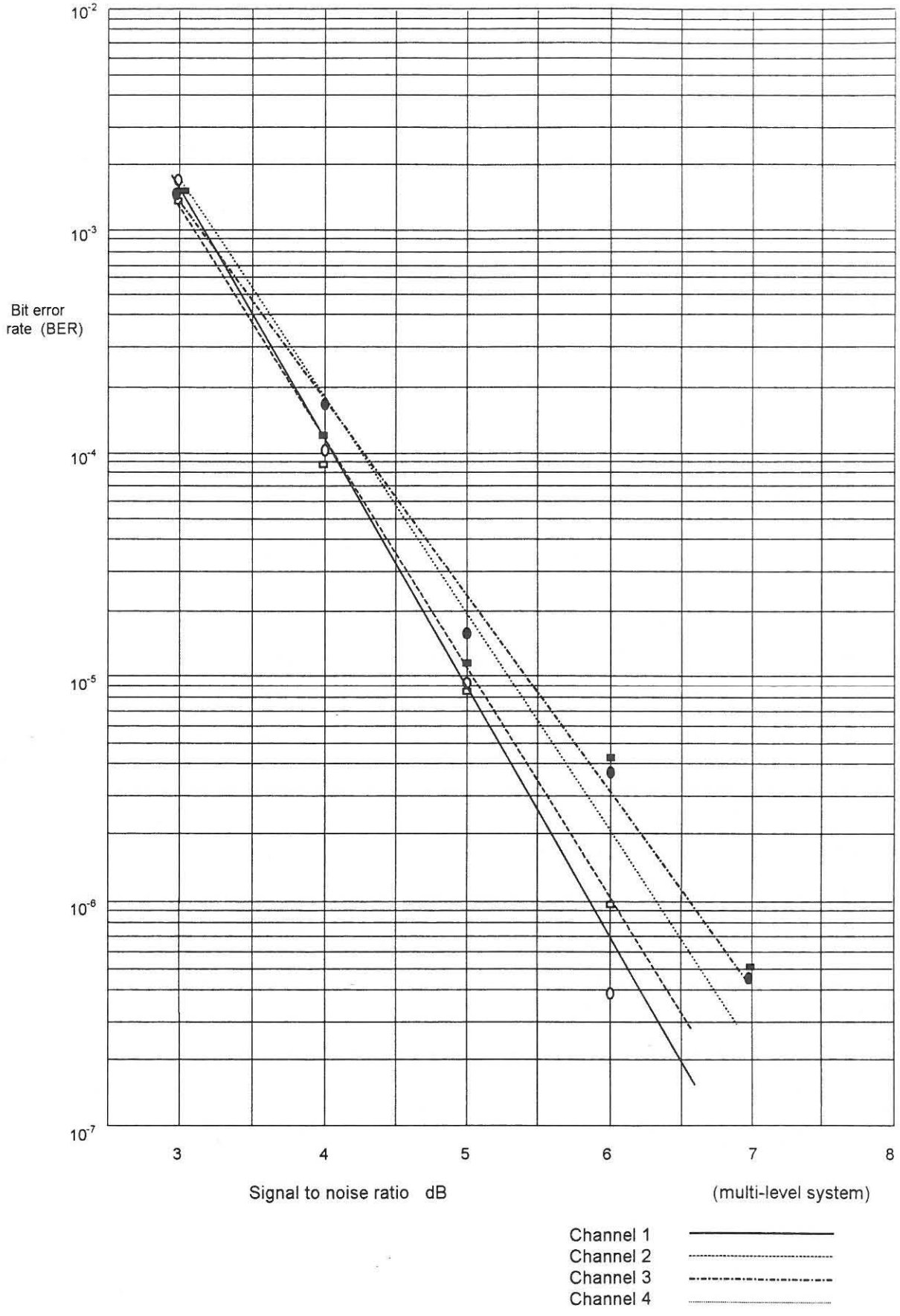


Fig.6 4 *BER in each channel for a cut-off frequency of 58,9kHz*

6.3 DISCUSSION OF TEST RESULTS FOR THE BINARY SYSTEM

The same set of tests were conducted on the binary system of sequency division multiplexing. Results of the bit error rate tests are presented in tables 4 to 6 in appendix C. The overall (total) bit error rate that was measured when the 22,5kHz, 27kHz and 58,9kHz low-pass filters were used in the line simulator is illustrated by the graphs in Fig.6.5.

The overall (total) bit error rate that was measured was the total number of errors for filter cut-off frequencies of 22,5kHz, 27kHz and 58,9 kHz are given in tables 6.4 to 6.6 and the graphs are presented in Fig. 6.5.

As for the multi-level system, the graphs show that there is a significant degradation of noise immunity when the frequency band is limited. This is evident by the spacing between the lines for the 58,9kHz, 27kHz and 22,5kHz filters. For example, at a signal to noise ratio of 7,0dB the BER worsens from about 10^{-6} to about 10^{-3} when the upper frequency limit is reduced from 58,9kHz to 27kHz.

Again, this degradation of noise immunity is to be expected as the filters introduce severe waveform distortion by suppressing harmonics and produce phase distortion as well. This will impair orthogonality of the signals in the four channels and results in cross talk between them leading to errors in the outputs of the four channels at the receiver [2, p. 233].

Bit error rates that were measured in each channel when the low-pass filters of 22,5kHz, 27kHz and 58,9kHz were inserted in the line simulator are given by the curves in Fig. 6.6, Fig.6.7 and Fig.6.8 respectively.

Inspection of the lines in Fig. 6.6 to Fig. 6.8 shows that the differences between the channels become more marked as the cut-off frequency is reduced. While only small differences between the channels are evident in Fig.6.8 for a cut-off frequency of 58,9kHz, considerable differences between the channels are indicated by the curves in Fig.6.6 for a filter cut-off frequency of 22,5kHz.

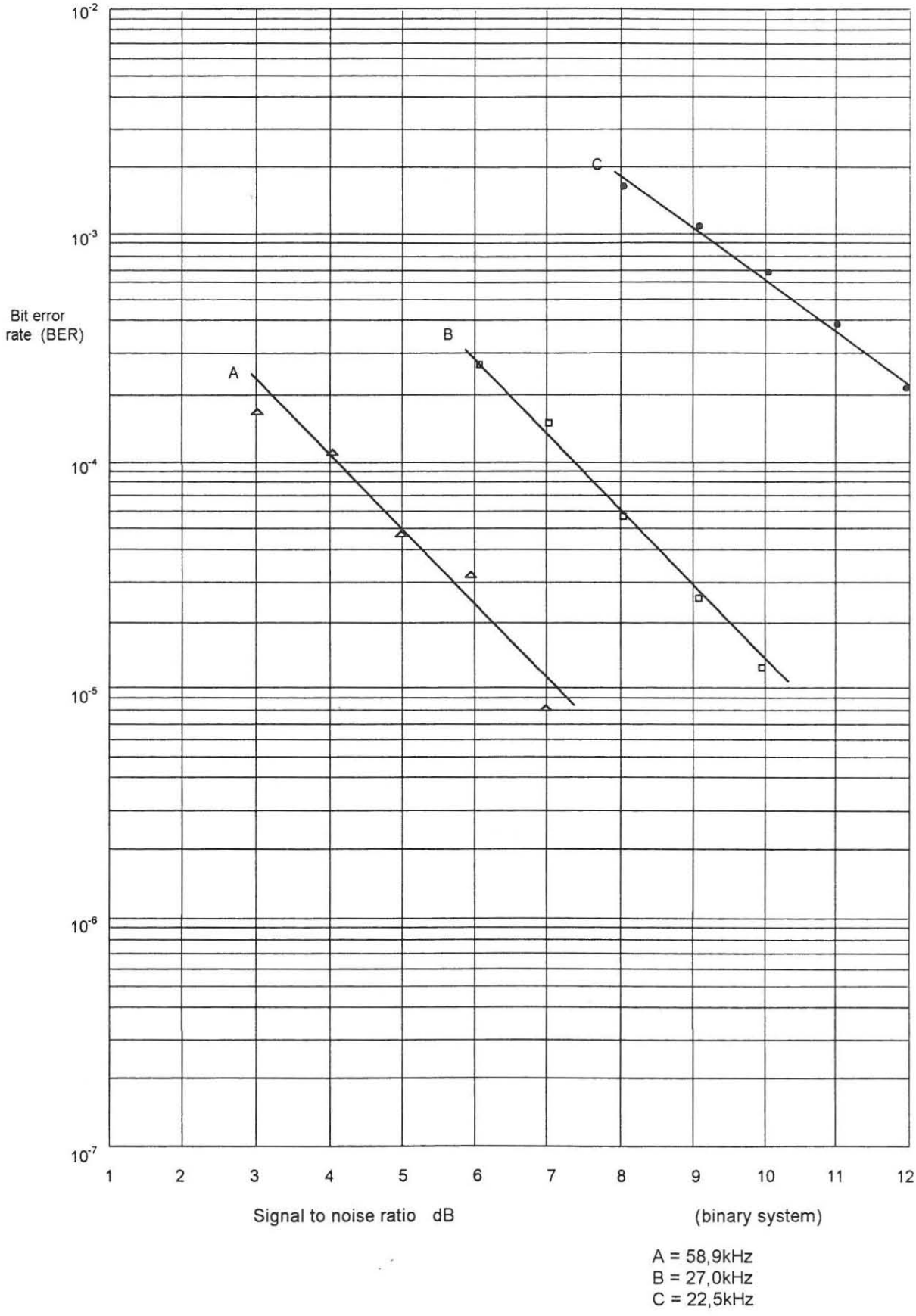


Fig. 6.5 *Overall BER for cut-off frequencies of 22,5kHz, 27kHz and 58,9kHz*

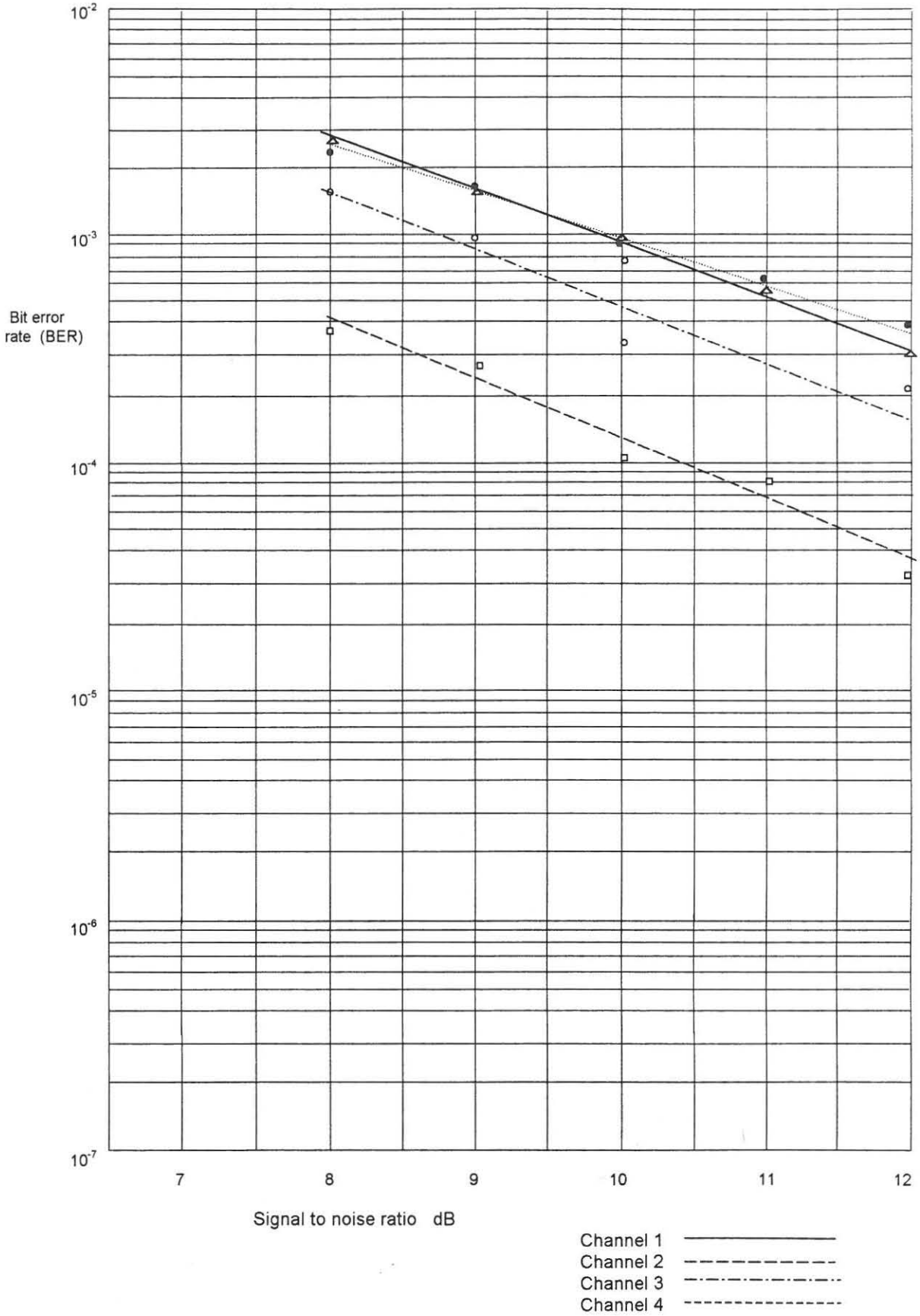


Fig. 6.6 *BER in each channel for a cut-off frequency of 22,5kHz*

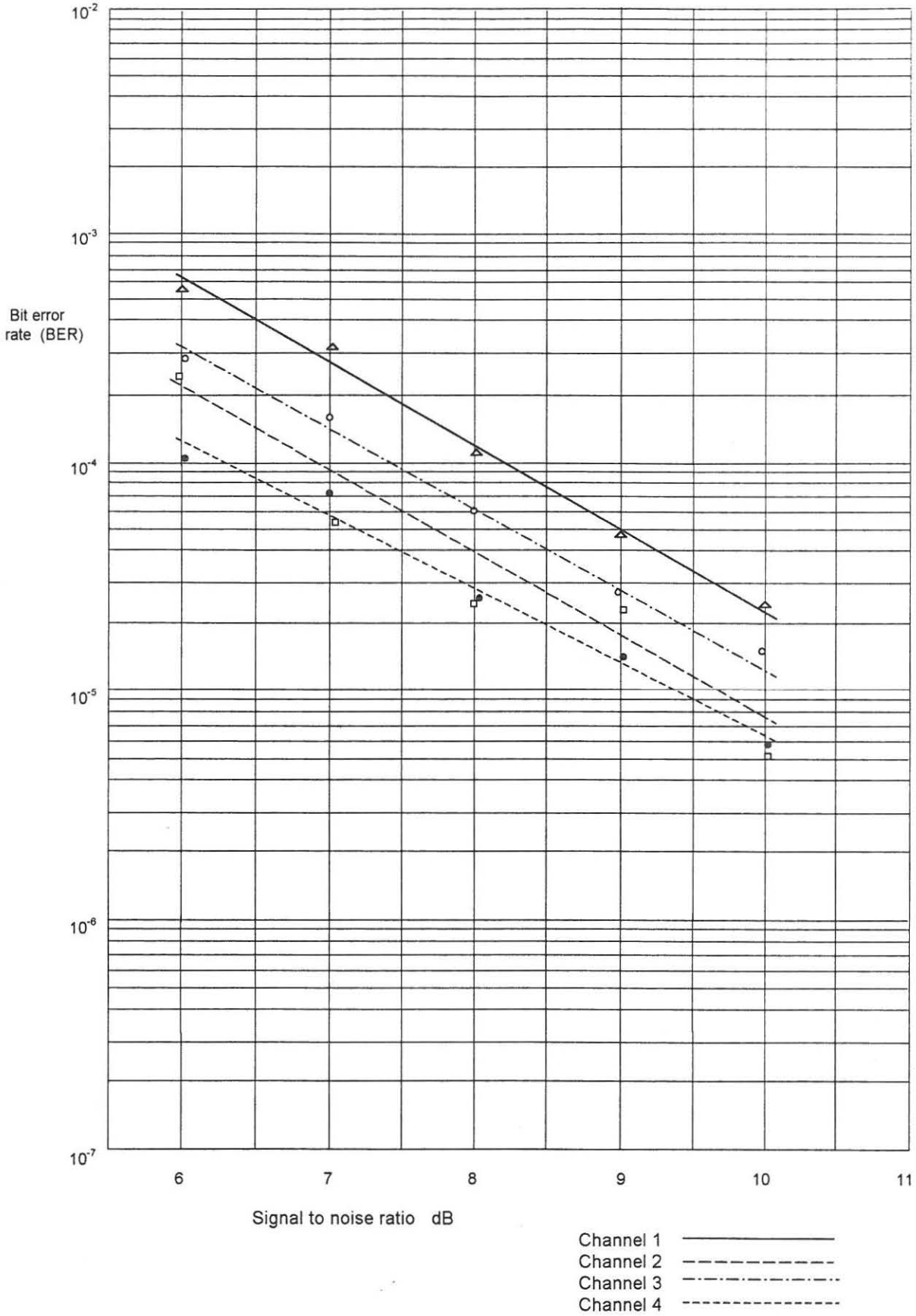


Fig.6.7 *BER in each channel for a cut-off frequency of 27,0kHz*

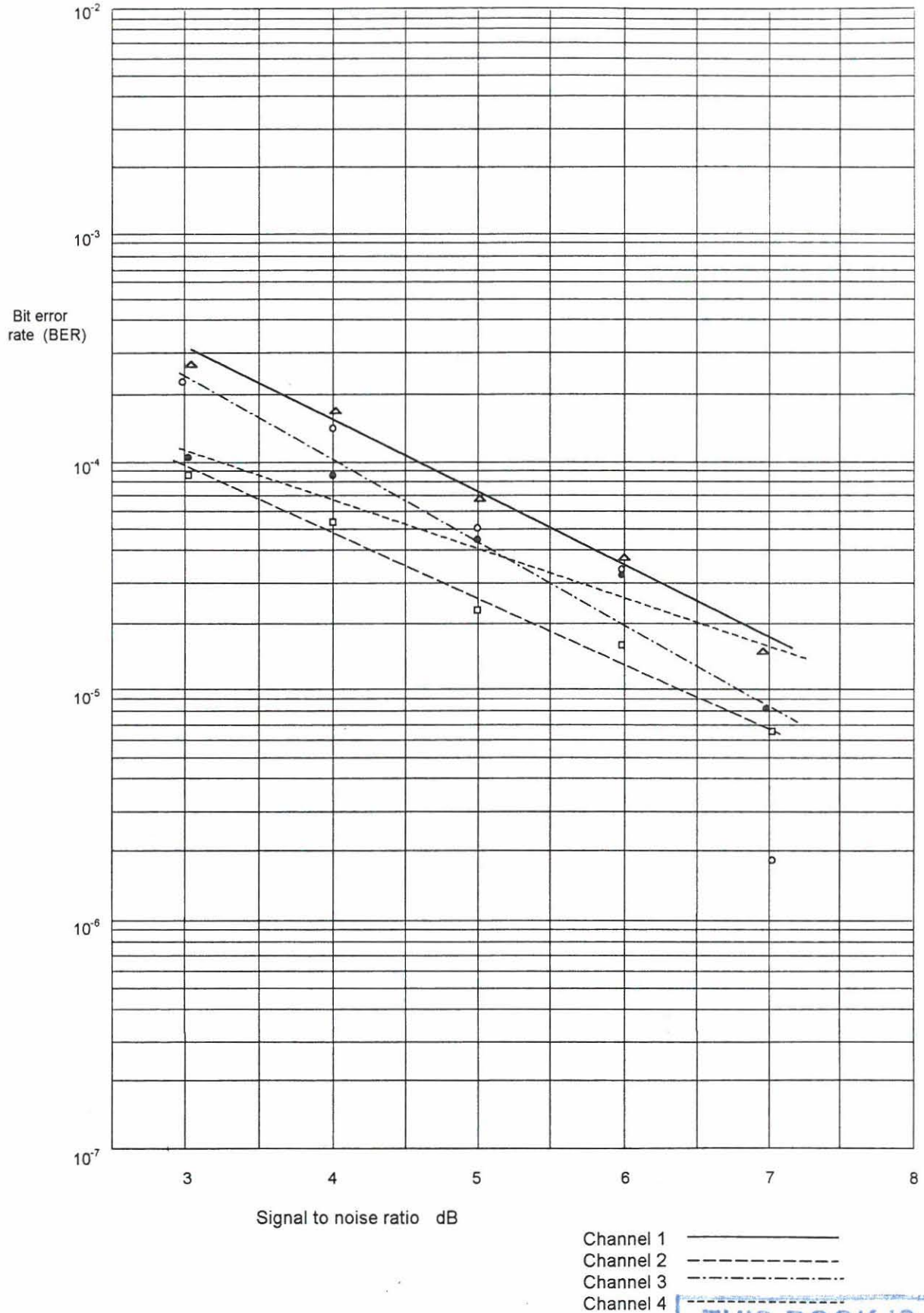


Fig.6.8 *BER in each channel for a cut-off frequency of 58,9kHz*

6.4 CONCLUSIONS

A four-channel, multi-level system of sequency division multiplexing has been designed, built and tested. This was followed by the design, construction and testing of a binary system of sequency division multiplexing. Both systems were found to operate satisfactorily and test results obtained are comparable with those obtained by Gordon, J. A. and Barrett, R. [8, p. 420].

It is suspected that differences between the signal-to-noise ratio performance of the four channels is mainly due to differences that arise in linear circuits employing analog techniques. These problems arise with manufacturing spread of components and setting up adjustments. For example, the data recovery filters in the two systems employ integrating circuits and the performance of these circuits is dependent upon tolerances in the component values and setting up adjustments.

From the results obtained it is clear that the performance of the binary system is superior to that of the multi-level system at high noise levels. However, contrary to expectations, the multi-level system test results appear to be better than those of the binary system for low levels of noise. Different results may be obtained by further experimentation with different signal levels and different types of low-pass filter. Another reason for this anomaly may be that the binary system requires a larger frequency band than the multi-level system. (See paragraph 5.4).

The slicing levels used in the binary system of SDM were chosen by inspection of the waveforms for each code combination. This approach would not be feasible for systems with a larger number of channels and some research into quantitative methods of selecting slicing levels would be required.

Since sequency division multiplexing requires the use of a relatively large frequency band it's applications at this stage may be limited to co-axial cable or other "wire type" of communication systems, or by using the UHF frequency band. The SDM system of multiplexing has a number of advantages over conventional techniques and it's use should be explored in, for example telemetry applications.

APPENDIX A

MathCAD SIMULATION

OF

MULTI-LEVEL SEQUENCY DIVISION MULTIPLEXING

The principles of multi-level sequency division multiplexing are illustrated using MathCAD.

Four carriers are used with four data inputs.

Sine wave functions are used to generate the first three Rademacher functions and these are used to produce the four Walsh carriers.

The data inputs of 1 and 0 modulate the carriers and the modulator outputs are combined resulting in a multi-level transmitted signal.

The multi-level signal is demodulated and the outputs are applied to integrator circuits to recover the original data signals.

A period of 2π with increments of 0.01π is used for the sinewaves.

$t := 0, .01 .. 2$

$a(t) := \sin(1 \cdot \pi \cdot t)$ $b(t) := \sin(2 \cdot \pi \cdot t)$ $c(t) := \sin(4 \cdot \pi \cdot t)$

Rad(1,t), Rad(2,t) and Rad(3,t) are produced from these sine waves using the if conditional as follows;

$R_1(t) := \text{if}(a(t) > 0, 1, -1)$

$R_2(t) := \text{if}(b(t) > 0, 1, -1)$

$R_3(t) := \text{if}(c(t) > 0, 1, -1)$

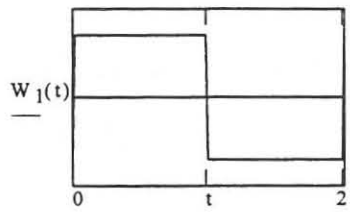
From the theory, Wal(1,t) = Rad(1,t), Wal(2,t) = Rad(1,t)*Rad(2,t) Wal(3,t) = Rad(2,t) and Wal(4,t) = Rad(2,t)*Rad(3,t)

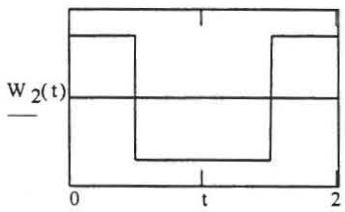
Then,

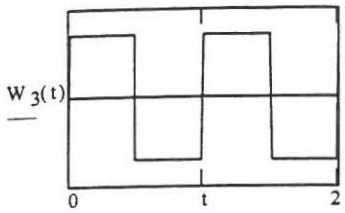
$W_1(t) := R_1(t)$ $W_2(t) := R_1(t) \cdot R_2(t)$

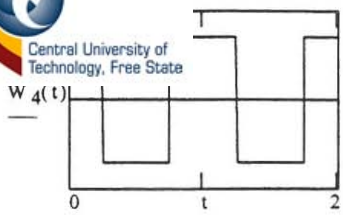
$W_3(t) := R_2(t)$ $W_4(t) := R_2(t) \cdot R_3(t)$

Waveforms of the four walsh functions are shown below;









The Walsh carriers must now be modulated by data.
With four carriers, there must be four data inputs.
These are d1, d2, d3 and d4.
Sixteen possible data combinations are tabulated below.

	d1	d2	d3	d4		d1	d2	d3	d4
1	0	0	0	0	9	1	0	0	0
2	0	0	0	1	10	1	0	0	1
3	0	0	1	0	11	1	0	1	0
4	0	0	1	1	12	1	0	1	1
5	0	1	0	0	13	1	1	0	0
6	0	1	0	1	14	1	1	0	1
7	0	1	1	0	15	1	1	1	0
8	0	1	1	1	16	1	1	1	1

Three of these data input combinations will be used to show how modulation, demodulation and signal recovery take place. The data combinations chosen for this purpose each have one, two, and three logic ones as shown below.

0 0 1 0
0 1 0 1
1 0 1 1

The combination 0 0 0 0 is not considered as the modulator outputs are all zero for this case. The combined signal output is also zero and each demodulator output is zero.

(1) DATA COMBINATION (0 0 1 0)

Each modulator output is the product of its Walsh carrier and the logic level of 1 or 0 at the data input.

MODULATOR 1 OUTPUT

$$M_1(t) = 0 \cdot W_1(t)$$

MODULATOR 2 OUTPUT

$$M_2(t) = 0 \cdot W_2(t)$$

MODULATOR 3 OUTPUT

$$M_3(t) = 1 \cdot W_3(t)$$

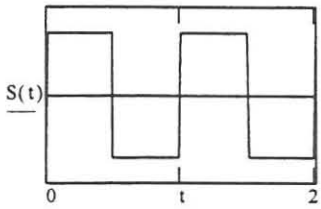
MODULATOR 4 OUTPUT

$$M_4(t) = 0 \cdot W_4(t)$$

TRANSMITTED SIGNAL

$$S(t) = M_1(t) + M_2(t) + M_3(t) + M_4(t)$$

The waveform of this signal is given.

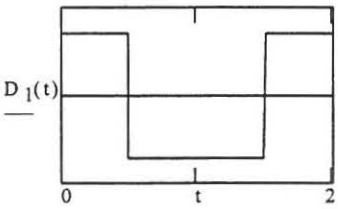


The output of each demodulator is the product of the received signal and its walsh carrier.

Since three different sets of data inputs are used to study the behaviour of the system, different sets of symbols are used for the signals in each of the cases.

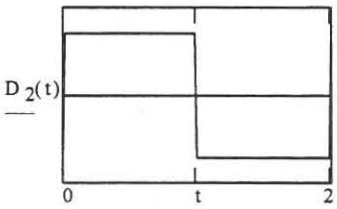
DEMODULATOR 1 OUTPUT

$$D_1(t) = S(t) \cdot W_1(t)$$



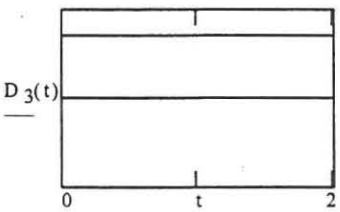
DEMODULATOR 2 OUTPUT

$$D_2(t) = S(t) \cdot W_2(t)$$



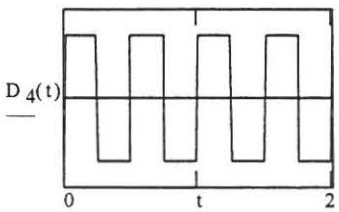
DEMODULATOR 3 OUTPUT

$$D_3(t) = S(t) \cdot W_3(t)$$



DEMODULATOR 4 OUTPUT

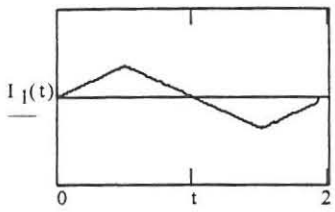
$$D_4(t) = S(t) \cdot W_4(t)$$



Each demodulator output is passed to an integrating circuit. At the end of the period of integration the level of the integrator output will determine whether a 1 or 0 bit is present.

INTEGRATOR 1 OUTPUT

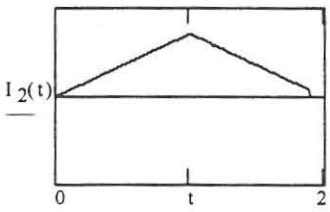
$$I_1(t) = \int_0^t D_1(t)\,dt$$



The integrator output is low representing a 0 bit.

INTEGRATOR 2 OUTPUT

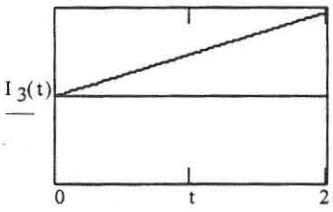
$$I_2(t) = \int_0^t D_2(t)\,dt$$



The integrator output is low representing a 0 bit.

INTEGRATOR 3 OUTPUT

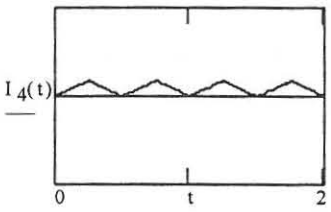
$$I_3(t) = \int_0^t D_3(t)\,dt$$



The integrator output is high representing a 1 bit.

INTEGRATOR 4 OUTPUT

$$I_4(t) = \int_0^t D_4(t)\,dt$$



The integrator output is low representing a 0 bit.

THE FOUR INTEGRATOR OUTPUTS CORRESPOND WITH THE FOUR DATA INPUTS.

(2) DATA COMBINATION (0 1 0

MODULATOR 1 OUTPUT

$N_1(t) = 0 \cdot W_1(t)$

MODULATOR 2 OUTPUT

$N_2(t) = 1 \cdot W_2(t)$

MODULATOR 3 OUTPUT

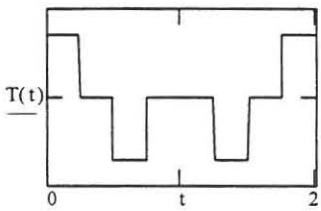
$N_3(t) = 0 \cdot W_3(t)$

MODULATOR 4 OUTPUT

$N_4(t) = 1 \cdot W_4(t)$

TRANSMITTED SIGNAL

$T(t) = N_1(t) + N_2(t) + N_3(t) + N_4(t)$

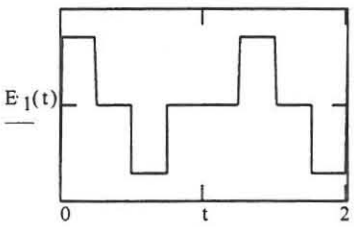


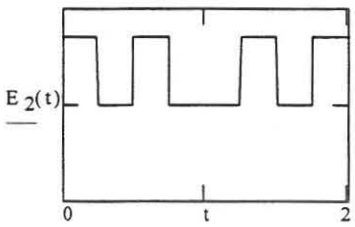
DEMODULATOR 1 OUTPUT

$E_1(t) = T(t) \cdot W_1(t)$

DEMODULATOR 2 OUTPUT

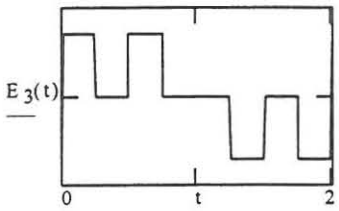
$E_2(t) = T(t) \cdot W_2(t)$





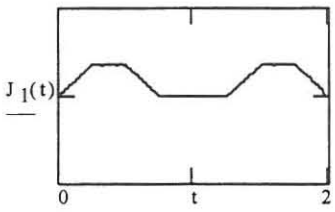
DEMODULATOR 3 OUTPUT

$$E_3(t) = T(t) \cdot W_3(t)$$



INTEGRATOR 1 OUTPUT

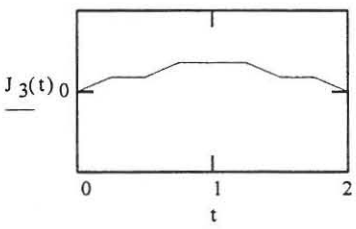
$$J_1(t) = \int_0^t E_1(t)\,dt$$



The integrator output is low representing a 0 bit

INTEGRATOR 3 OUTPUT

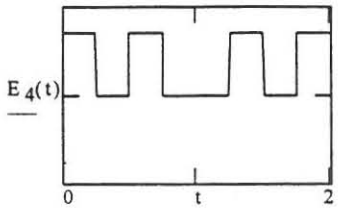
$$J_3(t) = \int_0^t E_3(t)\,dt$$



The integrator output is low representing a 0 bit

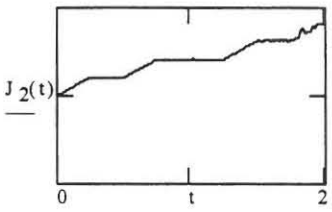
TOR 4 OUTPUT

$$E_4(t) = T(t) \cdot W_4(t)$$



INTEGRATOR 2 OUTPUT

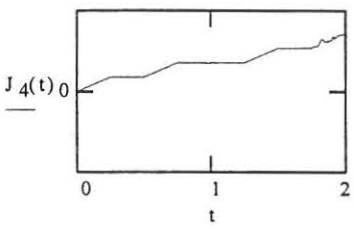
$$J_2(t) = \int_0^t E_2(t)\,dt$$



The integrator output is high representing a 1 bit

INTEGRATOR 4 OUTPUT

$$J_4(t) = \int_0^t E_4(t)\,dt$$



The integrator output is high representing a 1 bit

(3 DATA COMBINATION (1 0 1

MODULATOR 1 OUTPUT

$$P_1(t) = 1 \cdot W_1(t)$$

MODULATOR 2 OUTPUT

$$P_2(t) = 0 \cdot W_2(t)$$

MODULATOR 3 OUTPUT

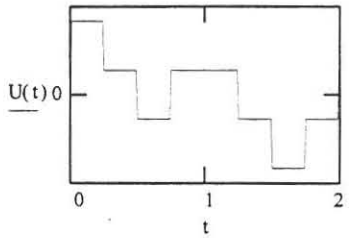
$$P_3(t) = 1 \cdot W_3(t)$$

MODULATOR 4 OUTPUT

$$P_4(t) = 1 \cdot W_4(t)$$

TRANSMITTED SIGNAL

$$U(t) = P_1(t) + P_2(t) + P_3(t) + P_4(t)$$

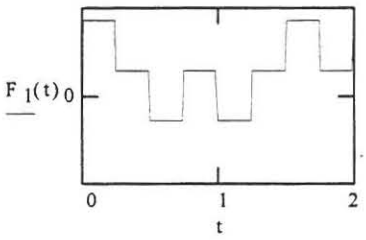


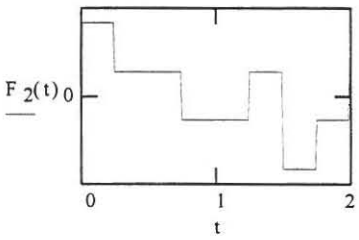
DEMODULATOR 1 OUTPUT

$$F_1(t) = U(t) \cdot W_1(t)$$

DEMODULATOR 2 OUTPUT

$$F_2(t) = U(t) \cdot W_2(t)$$



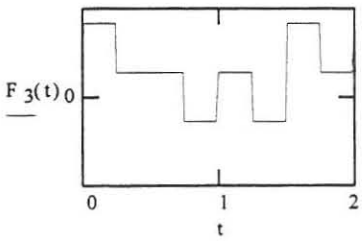


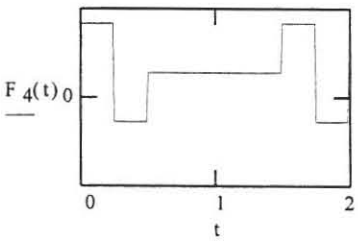
DEMODULATOR 3 OUTPUT

$$F_3(t) = U(t) \cdot W_3(t)$$

DEMODULATOR 4 OUTPUT

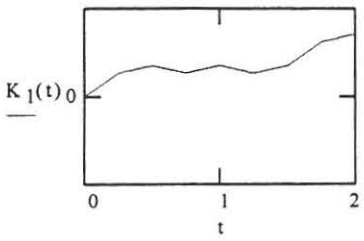
$$F_4(t) = U(t) \cdot W_4(t)$$





INTEGRATOR 1 OUTPUT

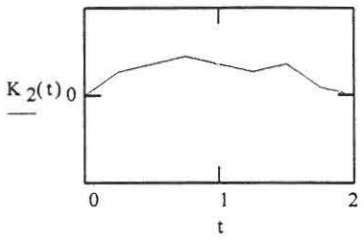
$$K_1(t) = \int_0^t F_1(t)\,dt$$



The integrator output is high representing a 1 bit.

R 2 OUTPUT

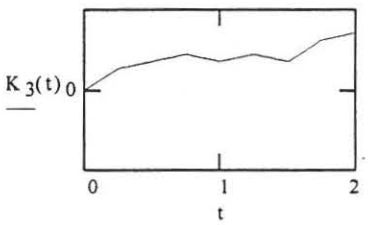
$$K_2(t) = \int_0^t F_2(t)\,dt$$



The integrator output is low representing a 0 bit.

INTEGRATOR 3 OUTPUT

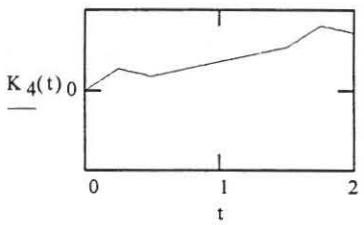
$$K_3(t) = \int_0^t F_3(t)\,dt$$



The integrator output is high representing a 1 bit.

INTEGRATOR 4 OUTPUT

$$K_4(t) = \int_0^t F_4(t)\,dt$$



The integrator output is high representing a 1 bit.

THE THREE MESSAGES HAVE BEEN TRANSMITTED AND RECEIVED SUCCESSFULLY .

==========

APPENDIX B

RESULTS OF TESTS

ON

RANDOM DATA GENERATOR

APPENDIX B

Test runs on random number generator.

Table 1 Test # 1

6	7	4	7	C	4	A	E	9	D	D	7	9
6	E	8	A	4	F	A	A	D	5	3	3	9
D	E	6	3	A	E	E	3	E	2	7	7	B
5	A	7	5	9	1	C	4	E	B	6	A	D
C	5	F	3	9	B	1	D	6	7	1	3	C
9	9	4	3	C	4	D	D	A	F	8	A	D
5	3	B	4	F	2	F	6	B	1	8	0	9
0	5	5	E	0	2	8	E	B	9	F	3	9
1	0	8	C	B	A	6	1	F	7	F	E	4
7	1	F	5	9	D	B	4	C	F	E	1	E
2	5	A	5	C	0	2	8	D	5	7	0	0
D	C	1	5	3	E	9	E	6	0	9	5	6
B	0	9	9	3	5	3	A	4	A	B	F	2
3	6	1	6	4	3	2	3	6	6	4	4	1
2	E	E	1	D	6	2	4	9	0	F	5	7
C	7	D	0	4	B	0	D	7	F	F	5	
6	9	C	A	B	0	F	D	7	5	B	B	
2	4	6	1	E	7	1	6	2	2	7	7	
8	5	5	3	B	1	4	7	4	8	3	6	
B	D	A	F	E	3	8	B	8	6	7	0	

Table 2 Test # 2

2	F	A	8	9	4	D	7	4	A	5	F
C	B	9	E	7	C	E	A	A	1	6	4
F	F	1	0	3	A	B	3	1	0	F	6
3	7	F	0	2	9	5	4	A	3	A	9
4	2	C	4	4	8	4	E	2	1	7	4
9	A	1	1	C	C	0	2	3	F	5	1
2	A	5	2	0	E	5	A	3	D	3	2
8	D	6	4	1	2	9	9	3	F	6	A
E	1	F	2	7	6	2	1	1	7	4	0
D	F	7	D	D	8	A	E	1	9	E	C
F	1	6	6	E	D	3	0	F	7	7	E
7	D	9	E	8	7	2	C	F	5	5	F
A	5	9	B	8	E	3	6	3	2	6	7
8	C	9	B	4	5	D	F	9	6	7	4
5	7	F	7	5	A	E	A	9	9	9	6
0	5	0	C	E	7	F	5	E	0	5	
D	B	0	1	4	B	4	A	F	7	9	
9	4	4	6	7	2	7	F	E	4	C	
C	6	3	4	8	9	5	6	A	7	6	
8	E	0	2	7	C	9	E	9	1	C	

Table 3 Test # 3

C	C	4	1	C	A	3	3	9	C	3	D	2
0	7	F	3	7	2	1	C	6	0	B	5	6
D	4	6	6	E	B	5	B	1	C	F	C	F
B	9	8	1	A	F	C	0	2	9	1	B	F
D	6	1	2	B	2	1	4	5	2	0	5	7
B	8	5	A	8	0	6	F	0	5	6	A	9
2	E	C	F	C	8	6	C	2	E	E	0	4
8	4	0	F	D	C	D	8	5	1	D	7	7
E	3	7	F	F	D	8	7	F	8	A	C	2
3	7	B	9	4	3	A	5	F	A	9	E	5
0	8	2	5	B	9	4	1	B	1	4	8	9
A	0	B	A	B	7	2	6	8	F	E	9	1
F	7	F	1	6	E	3	A	8	3	1	8	7
E	8	6	A	3	1	9	3	E	2	7	D	0
1	D	3	E	2	7	E	B	0	4	A	0	C
A	A	4	8	8	7	F	E	1	0	3	0	
B	3	2	2	3	E	D	D	4	8	9	5	
3	7	2	8	F	9	9	D	D	9	2	1	
6	3	A	E	1	8	9	4	C	E	6	E	
4	D	C	3	D	5	4	B	5	2	1	A	

APPENDIX C

BIT ERROR RATE TEST RESULTS

TABLES C.1 TO C.6

APPENDIX C

Multi-level system

Table C.1 *Channel errors with filter cut-off frequency = 22,5 kHz.*

s/n ratio (dB)	8	9	10	11	12
Channel 1	477	166	50	18	10
Channel 2	2542	1132	352	97	21
Channel 3	1829	792	255	73	49
Channel 4	6597	3480	1392	612	286
Sum	11445	5570	2049	800	366
Total counter	11439	5563	2048	797	366

Table C.2 *Channel errors with filter cut-off frequency = 27 kHz.*

s/n ratio (dB)	6	7	8	9	10
Channel 1	1201	316	129	28	6
Channel 2	2527	1626	408	79	37
Channel 3	4354	2484	689	137	63
Channel 4	5169	2154	871	97	48
Sum	13251	6580	2097	341	154
Total counter	13229	6577	2093	341	153

Table C.3 *Channel errors with filter cut-off frequency = 58,9 kHz.*

s/n ratio (dB)	3	4	5	6	7
Channel 1	3451	220	21	1	0
Channel 2	3041	195	19	2	1
Channel 3	3183	373	33	8	1
Channel 4	3326	236	25	9	1
Sum	13001	1024	97	20	4
Total counter	12990	1024	97	20	4

Binary system

Table C.4 *Channel errors with filter cut-off frequency = 22,5 kHz.*

s/n ratio (dB)	8	9	10	11	12
Channel 1	5 177	3481	2 052	1 182	654
Channel 2	756	547	231	175	69
Channel 3	3 234	2 179	1 722	693	241
Channel 4	4 963	3 452	1 957	1 332	853
Sum	14 130	9 659	5 962	3 382	1817
Total counter	14 121	9 653	5 955	3 377	1812

Table C.5. *Channel errors with filter cut-off frequency = 27 kHz.*

s/n ratio (dB)	6	7	8	9	10
Channel 1	1 198	671	255	102	52
Channel 2	281	119	49	45	12
Channel 3	642	348	131	54	27
Channel 4	219	156	56	28	13
Sum	2 340	1 294	491	229	104
Total counter	2 334	1 290	488	227	103

Table C.6. *Channel errors with filter cut-off frequency = 58,9 kHz.*

s/n ratio (dB)	3	4	5	6	7
Channel 1	563	391	150	83	33
Channel 2	176	120	48	34	15
Channel 3	472	287	109	78	4
Channel 4	216	185	102	71	17
Sum	1 427	983	409	266	69
Total counter	1 418	979	406	265	69

APPENDIX D

FREQUENCY SPECTRA OF SDM SIGNALS

Frequency spectra of SSK signals

$t := 0 \ldots 255$

$j := 0 \ldots 64$

Generation of Wal(1,t)

$w_t := \sin\left[12 \cdot \pi \cdot \frac{t}{128}\right]$

Carrier

$a_t := \text{if}[w_t > 0, 1, -1]$

Frequency spectrum

$A := \text{fft}(a)$

Generation of Wal(2,t)

$x_t := \sin\left[12 \cdot \pi \cdot \frac{t}{128} + \frac{\pi}{2}\right]$

Carrier

$b_t := \text{if}[x_t > 0, 1, -1]$

Frequency spectrum

$B := \text{fft}(b)$

Generation of Wal(3,t)

$y_t := \sin\left[24 \cdot \pi \cdot \frac{t}{128}\right]$

Carrier

$c_t := \text{if}[y_t > 0, 1, -1]$

Frequency spectrum

$C := \text{fft}(c)$

Generation of Wal(4,t)

$z_t := \sin\left[24 \cdot \pi \cdot \frac{t}{128} + \frac{\pi}{2}\right]$

Carrier

$d_t := \text{if}[z_t > 0, 1, -1]$

Frequency spectrum

$D := \text{fft}(d)$

Generation of data g

$p_t := \sin\left[6 \cdot \pi \cdot \frac{t}{128}\right]$

Data pulses

$g_t := \text{if}[p_t > 0, 1, 0]$

Frequency spectrum

$G := \text{fft}(g)$

(1) Modulation of Wal(1,t) by data g

The data pulses, g, simply turn the carrier, Wal(1,t), on and off.

Modulated signal

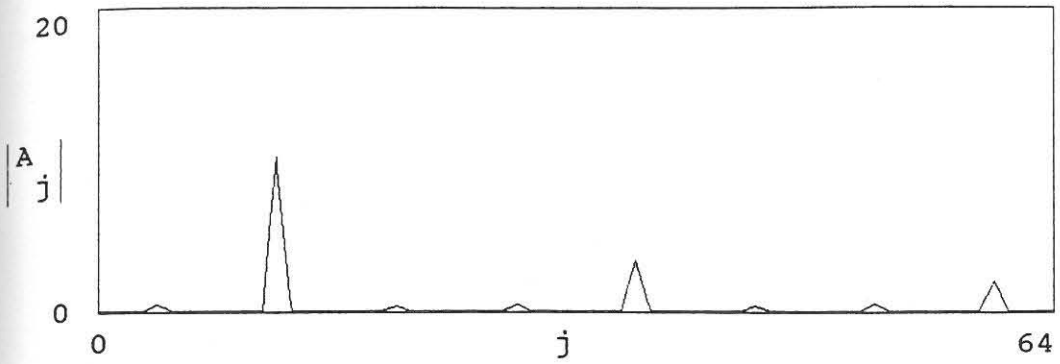
$m1_t := \text{if}[g_t > 0, a_t, 0]$

Frequency spectrum

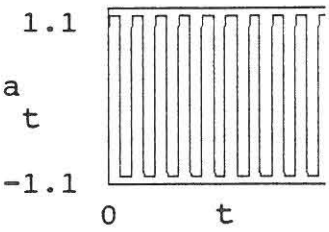
$M1 := \text{fft}(m1)$

In this case the duration of the data pulses is twice that of the Walsh function Wal(1,t).

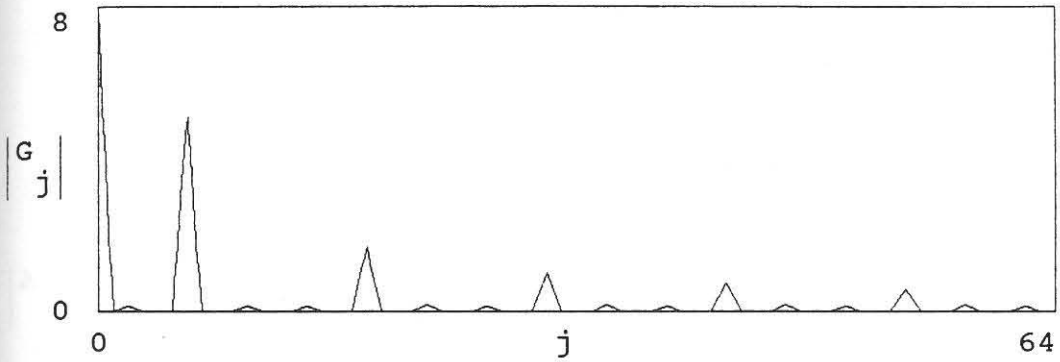
Frequency spectrum of carrier, Wal(1,t)



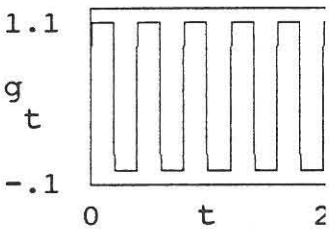
Carrier,Wal(1,
(Time domain)



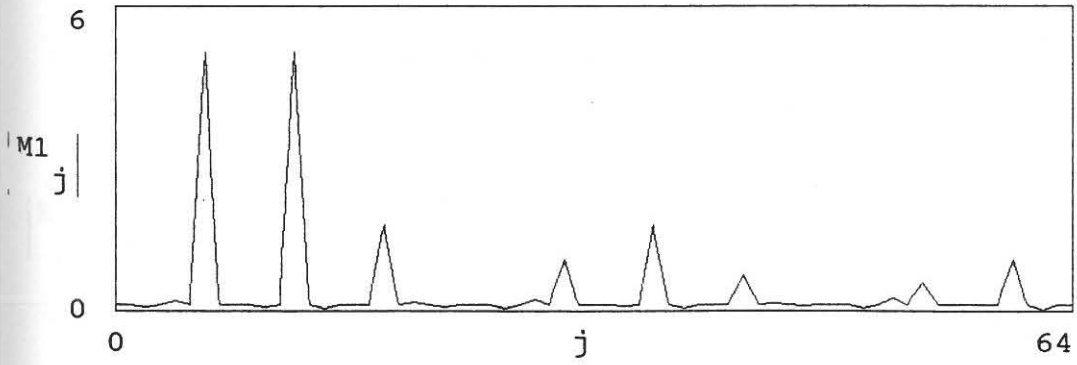
Frequency spectrum of data, G



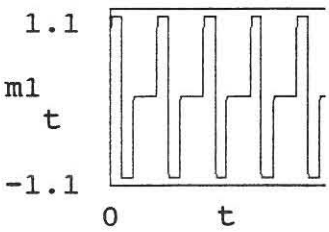
Data pulses



Frequency spectrum of modulated carrier



Modulated
carrier



Generation of data h

$q_t := \sin\left[4 \cdot \pi \cdot \frac{t}{128}\right]$

Data pulses

$h_t := if[q_t > 0, 1, 0]$

Frequency spectrum

H := fft(h)

(2) Modulation of Wal(1,t) by data h

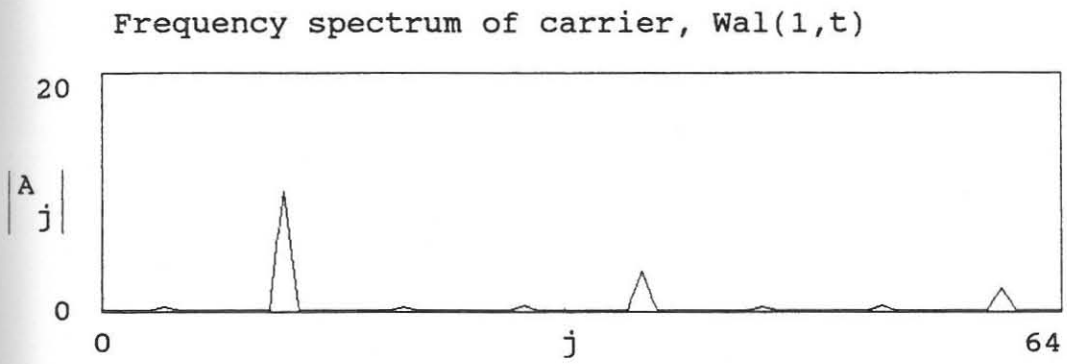
Modulated signal

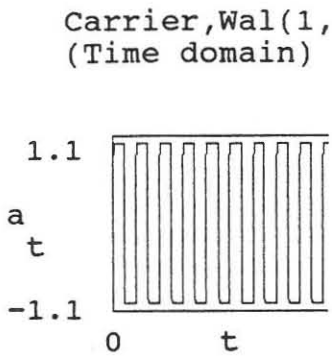
$m2_t := if[h_t > 0, a_t, 0]$

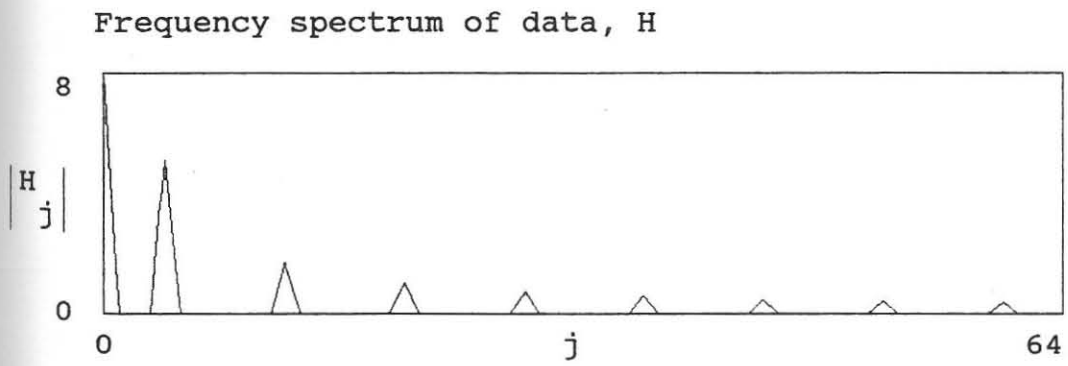
Frequency spectrum

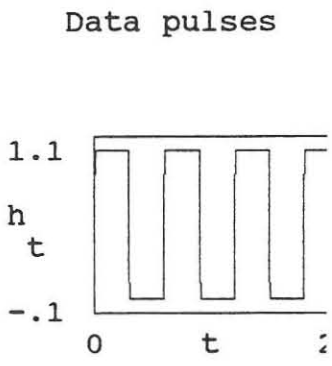
M2 := fft(m2)

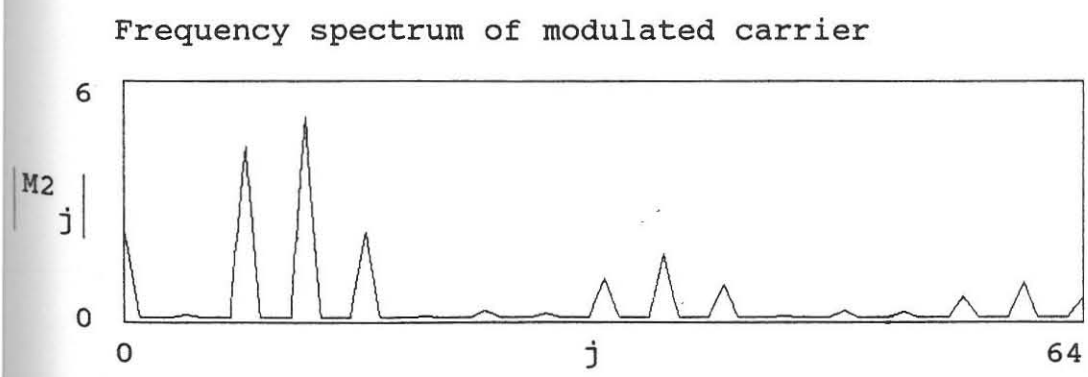
In this case the duration of the data pulses is three times that of the Walsh function Wal(1,t).

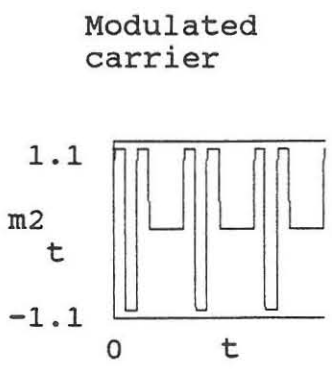












Generation of data i

$r_t := \sin\left[3 \cdot \pi \cdot \frac{t}{128}\right]$

Data pulses

$i_t := \text{if}[r_t > 0, 1, 0]$

Frequency spectrum

I := fft(i)

(2) Modulation of Wal(1,t) by data i

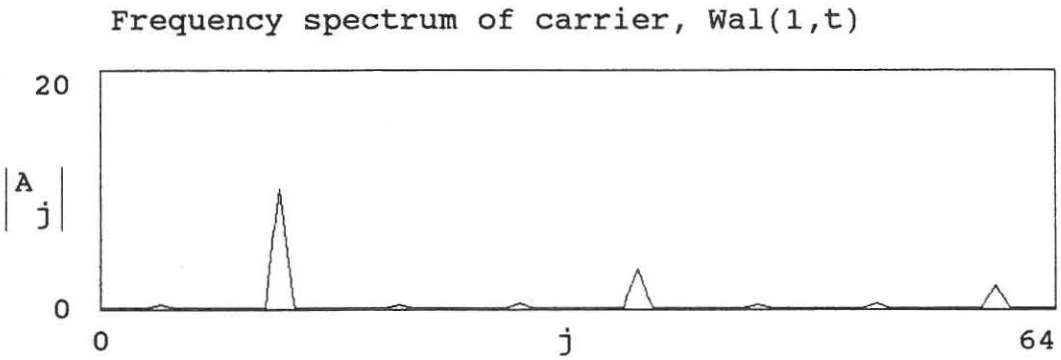
Modulated signal

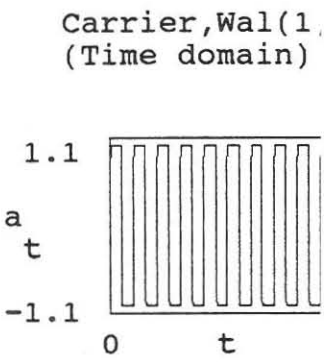
$m3_t := \text{if}[i_t > 0, a_t, 0]$

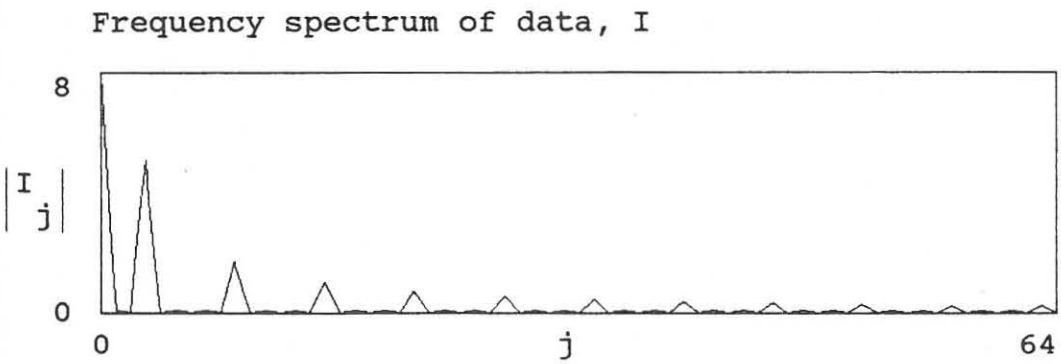
Frequency spectrum

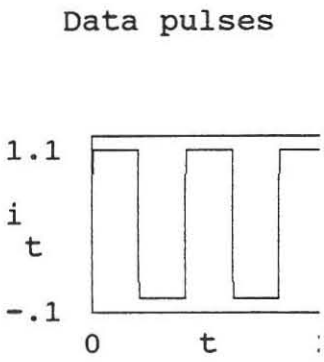
M3 := fft(m3)

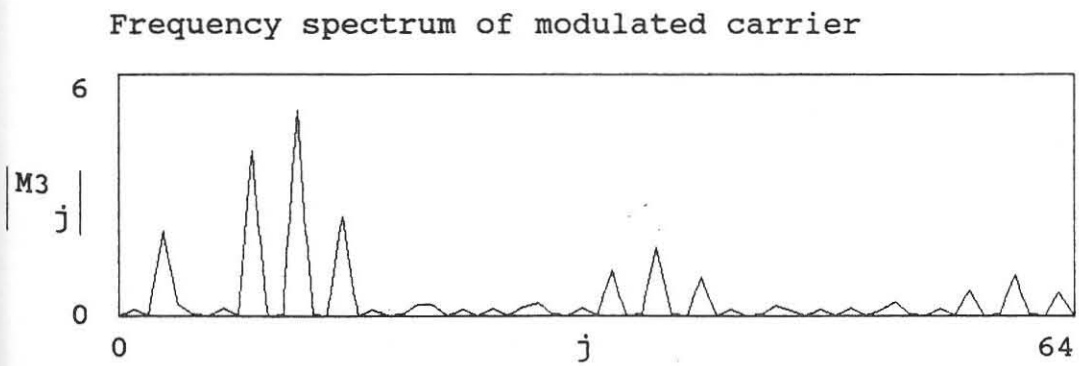
In this case the duration of the data pulses is four times that of the Walsh function Wal(1,t).

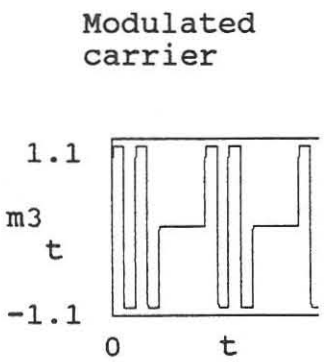












Frequency spect__ __ ____ signals

t := 0 ..255

Generation of Wal(1,t)

$$w_t := \sin\left[12\cdot\pi\cdot\frac{t}{128}\right]$$

Carrier

$$a_t := if\left[w_t < 0,1,0\right]$$

Frequency spectrum

g := fft(a)

j := 0 ..64

Generation of Wal(2,t)

$$x_t := \sin\left[12\cdot\pi\cdot\frac{t}{128} + \frac{\pi}{2}\right]$$

Carrier

$$b_t := if\left[x_t > 0,1,0\right]$$

Generation of Wal(3,t)

$$y_t := \sin\left[24\cdot\pi\cdot\frac{t}{128}\right]$$

Carrier

$$c_t := if\left[y_t < 0,1,0\right]$$

Generation of Wal(4,t)

$$z_t := \sin\left[24\cdot\pi\cdot\frac{t}{128} + \frac{\pi}{2}\right]$$

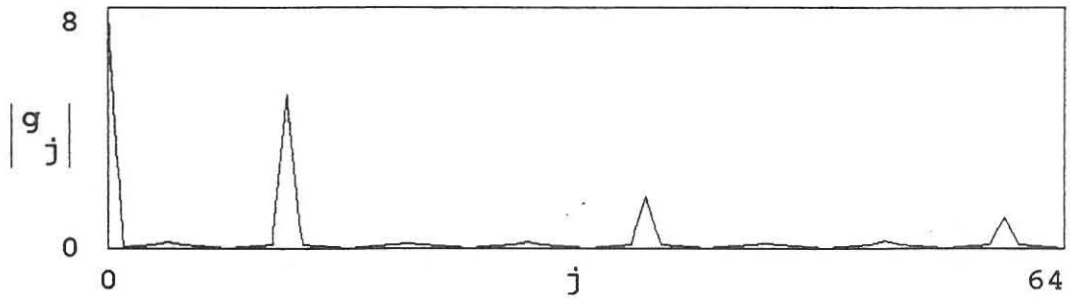
Carrier

$$d_t := if\left[z_t > 0,1,0\right]$$

The carriers used in the binary system switch between 0 and 1. When modulated by a "1" the "NOR" function is applied. In the simulation this is achieved by changing from > to < in the "if" statement for the carrier.

In this example the carriers Wal(1,t) and Wal(3,t) are modulated by 1's. The modulator outputs are then summed and sliced.

The sum component and the sliced signal are displayed in the time domain. The frequency spectrum of the sliced signal is also given.

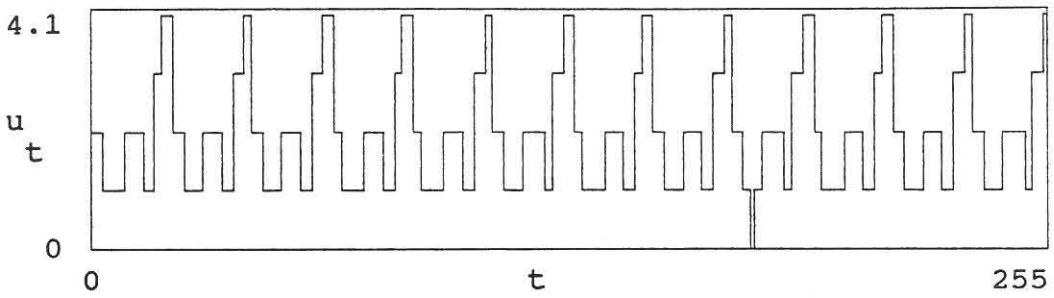


Frequency spectrum of Wal(1,t)

Sum of modulator outputs

$u_t := a_t + b_t + c_t + d_t$

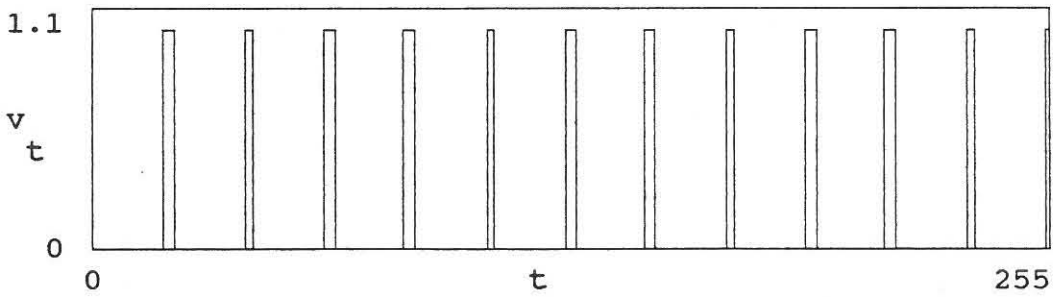
Multi-level signal



Set slicer at 3.7

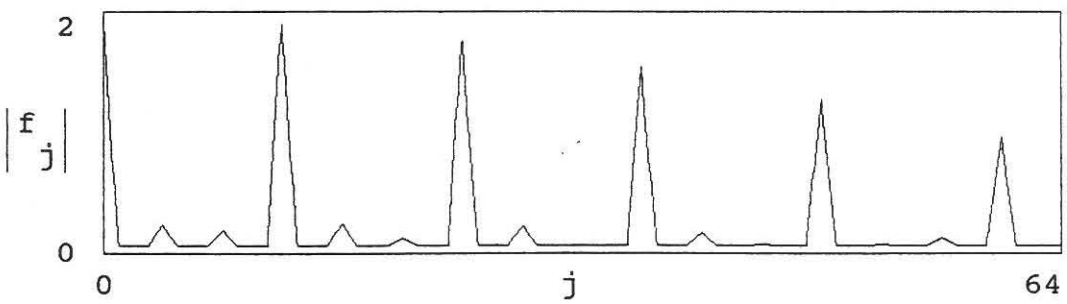
$v_t := if[u_t > 3.7, 1, 0]$

Sliced signal



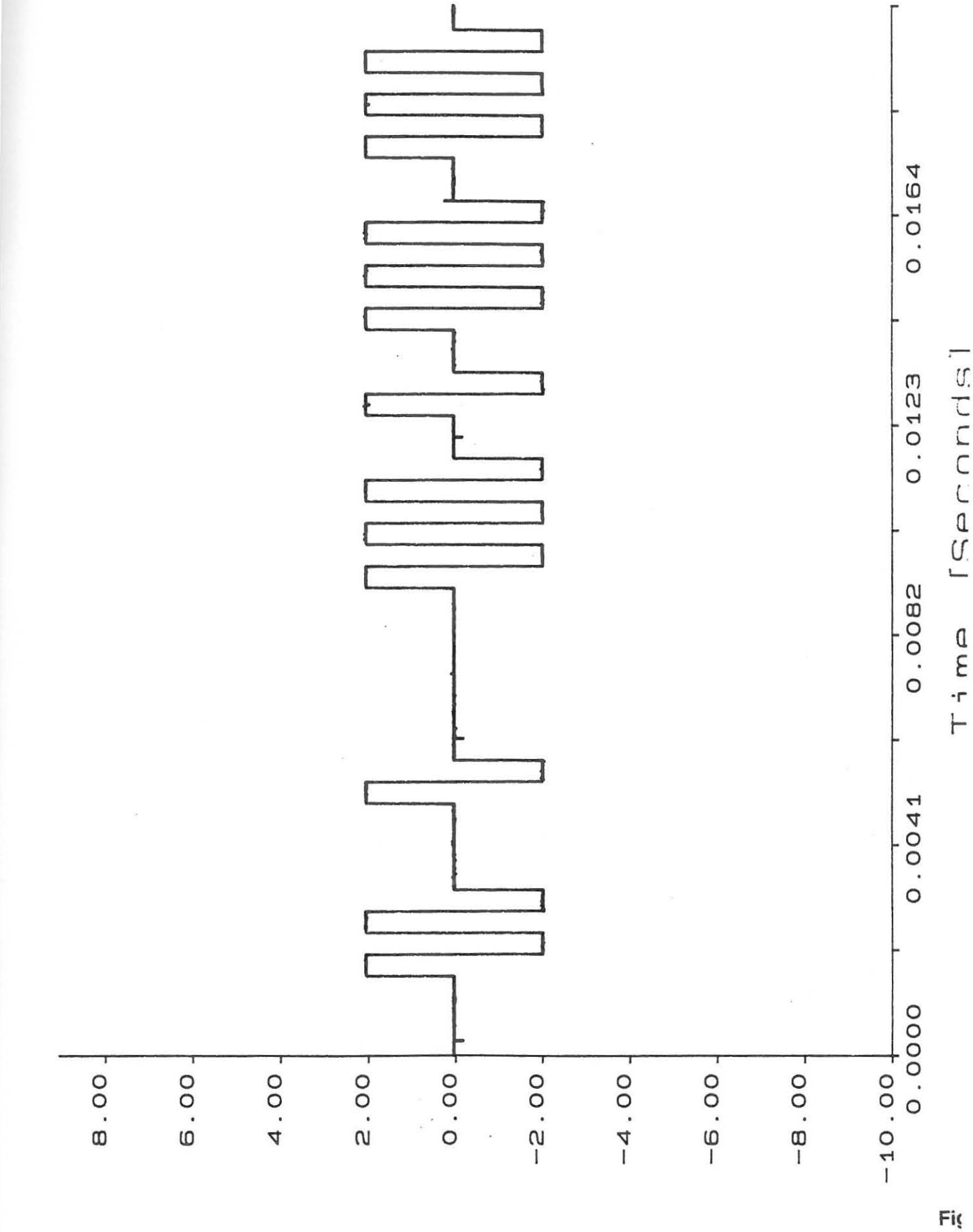
Frequency spectrum

f := fft(v)



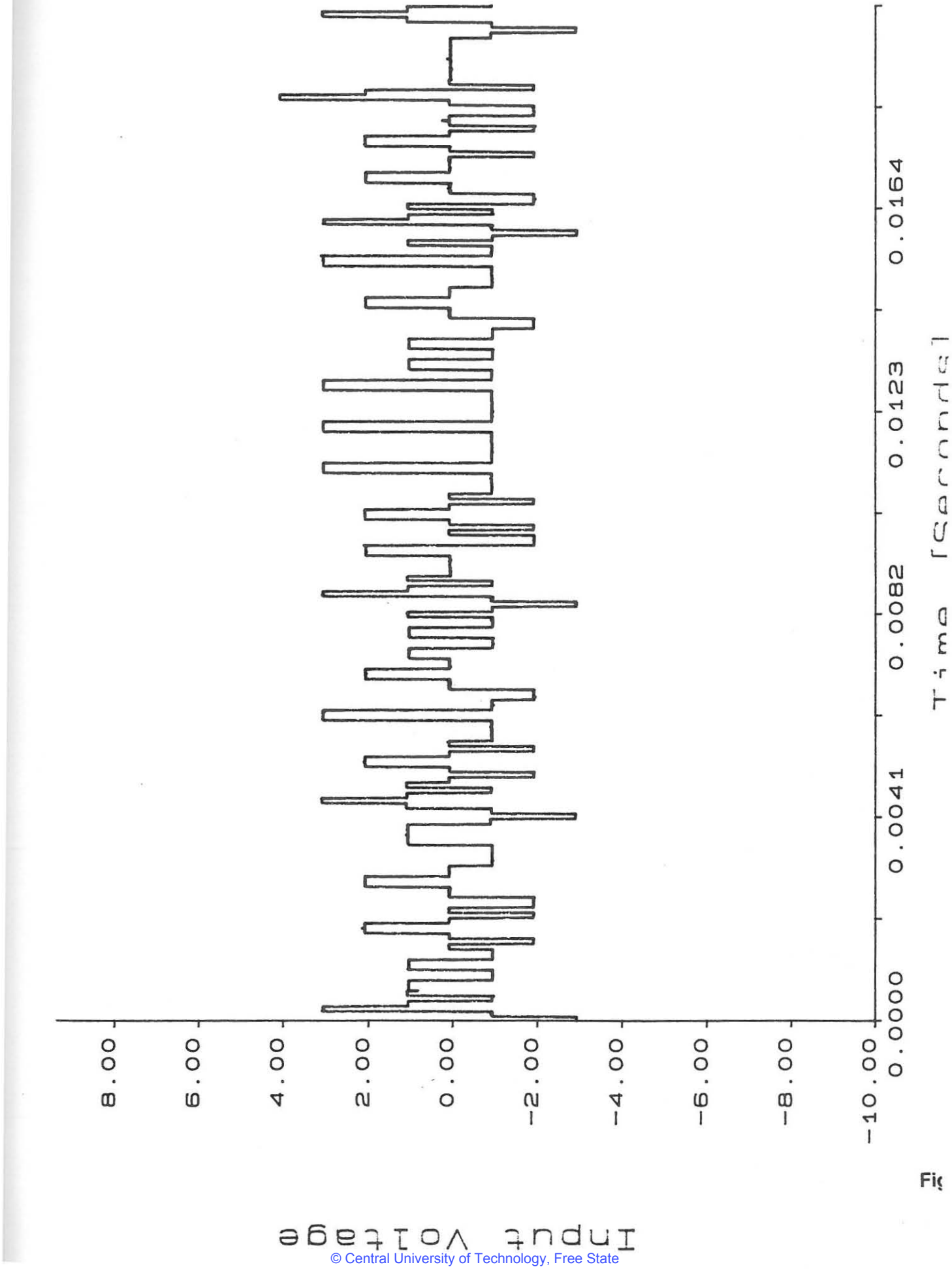
APPENDIX E

MEASUREMENTS OF WAVEFORMS AND FREQUENCY SPECTRA

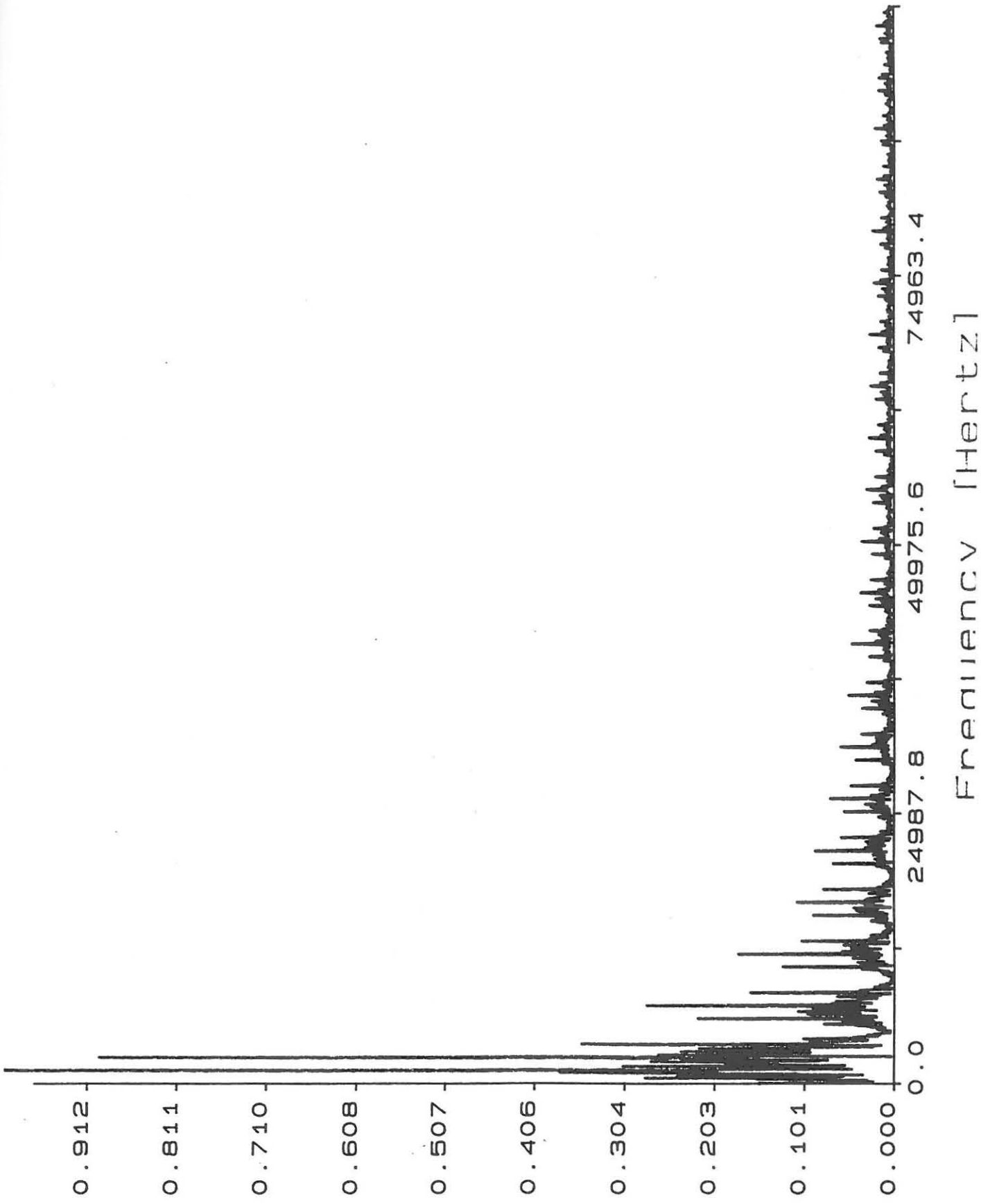


Fig

Fi



Fig



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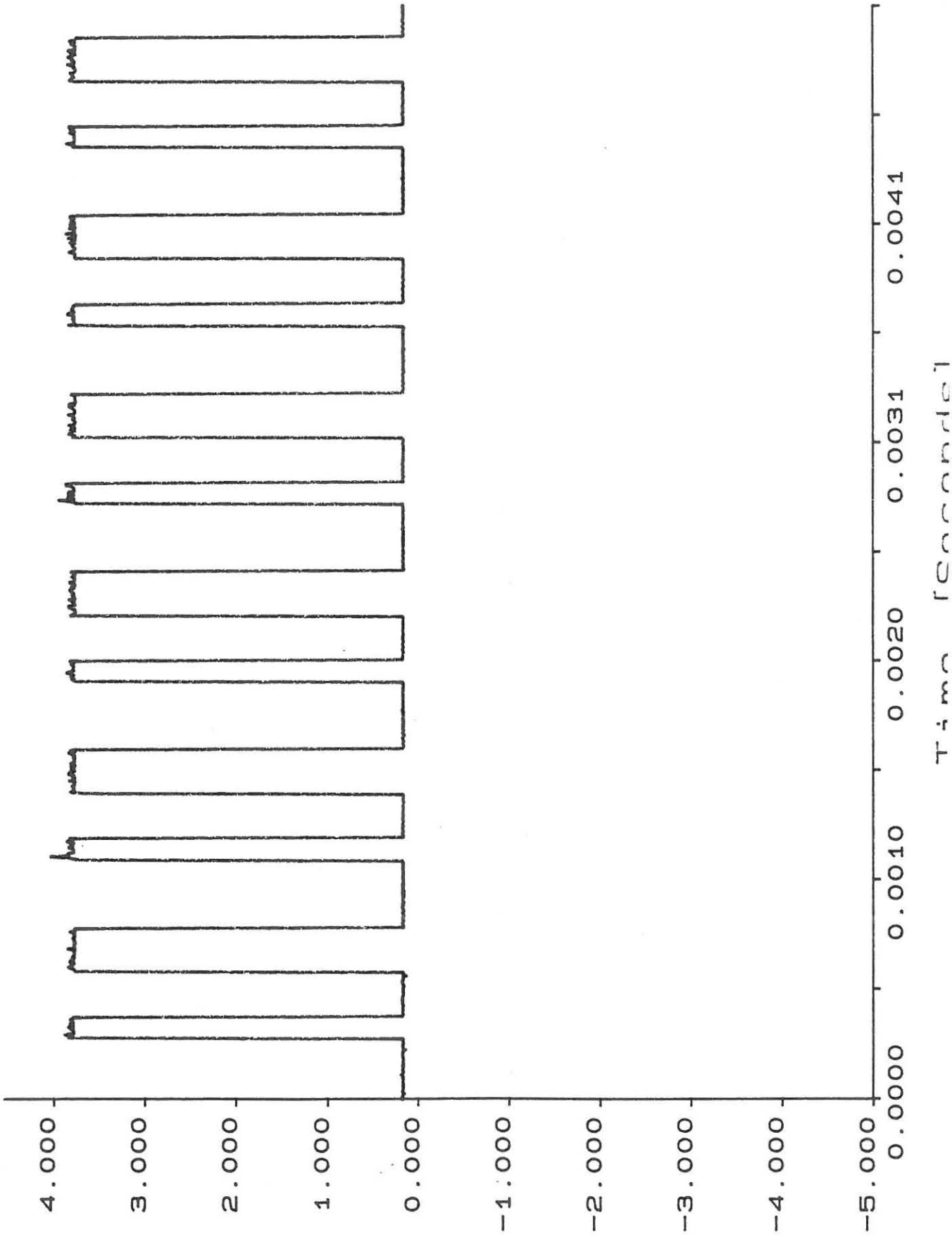

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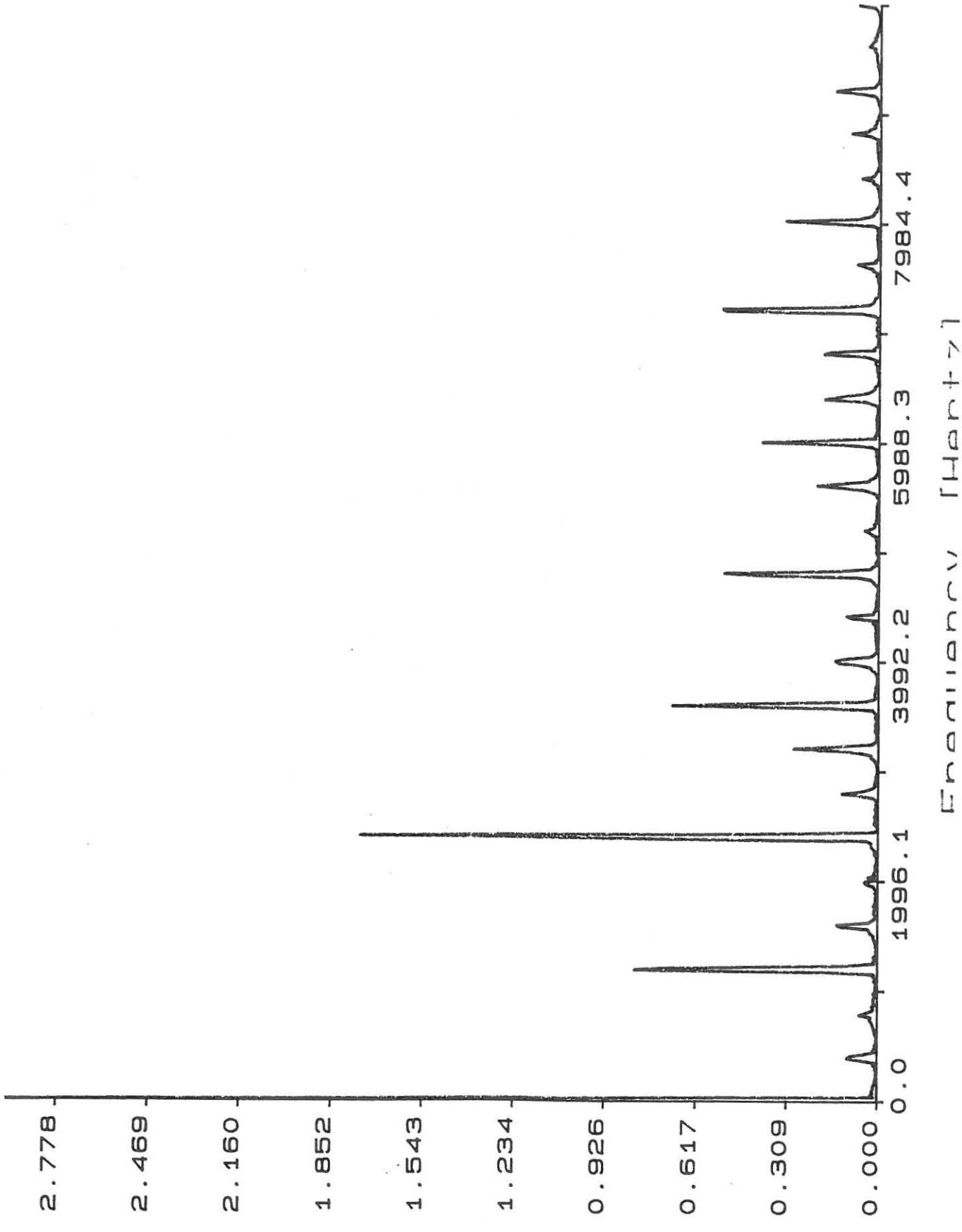

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APPENDIX F

SEQUENCY DIVISION MULTIPLEXING TECHNIQUES FOR THE TRANSMISSION OF DIGITAL INFORMATION

PAPER PRESENTED AT A CONFERENCE OF

THE SOCIETY OF ELECTRICAL AND ELECTRONIC EDUCATORS

UNIVERSITY OF PRETORIA

FEBRUARY 1995

SEQUENCY DIVISION MULTIPLEXING TECHNIQUES FOR THE TRANSMISSION OF DIGITAL INFORMATION

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ABSTRACT

This paper describes the principles of operation of multi-level and binary sequency division equipment which has been built at Technikon OFS. The technique of slicing the multi-level signal to produce binary signals differs somewhat from existing methods.

1. INTRODUCTION

The multiplexing of digital signals in telemetry and data transmission applications is usually performed with frequency or time division techniques. Modulation techniques such as frequency shift keying (fsk) or phase shift keying (psk) are used to impress data onto the carriers before transmission.

This paper describes two methods of sequency division multiplexing of digital signals using Walsh functions as carrier waves. Multi-level signalling is employed in the first method, while the second uses binary signalling.

Complete sets of transmitting and receiving equipment for both methods of sequency division multiplexing have been constructed, each with four channels operating at a signalling speed of 2400 bits per second.

2. WALSH FUNCTIONS:

The set of functions developed by J L Walsh in 1923 is a set of orthogonal waveforms. While a number of different sets of orthogonal functions are suitable for multiplexing applications, the only set which is as efficient as the sinusoidal functions in terms of bandwidth utilization are the Walsh functions (Beauchamp, 1984: 235)

A set of eight Walsh functions are shown in fig. 1.

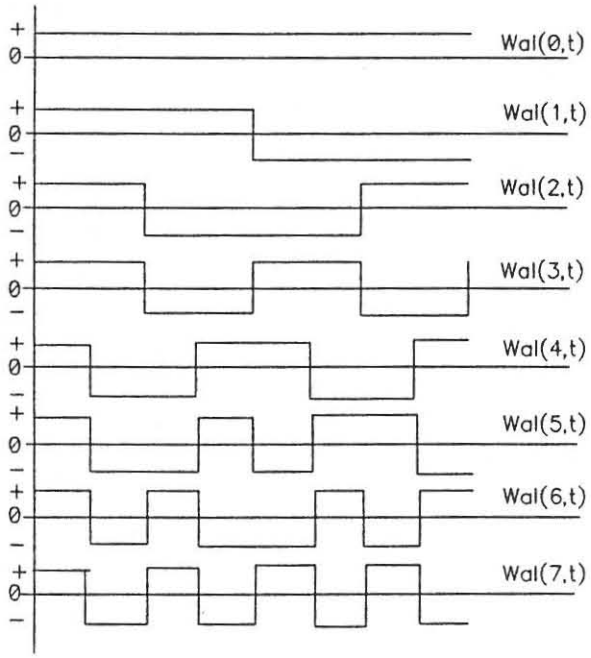

Fig.1.Walsh functions.

The first wave Wal(0,t) is simply a continuous dc signal with magnitude +1, while the rest of the waveforms switch between +1 and -1. An examination of Wal(5,t) and Wal(6,t) reveals that the "frequency" of these waveforms is not constant and the term frequency is therefore not appropriate. Instead, the term "sequency" is used to denote one half the average number of zero crossings (or sign changes) per unit time. (Tzafestas, 1985:8)

A set of four Walsh functions, W(1,t), W(2,t), W(3,t) and W(4,t) was used as carrier waveforms in the multi-level sequency division multiplexing system which was constructed.

The Walsh functions were produced by suitable combinations of block pulse functions. The process is illustrated in fig 2.

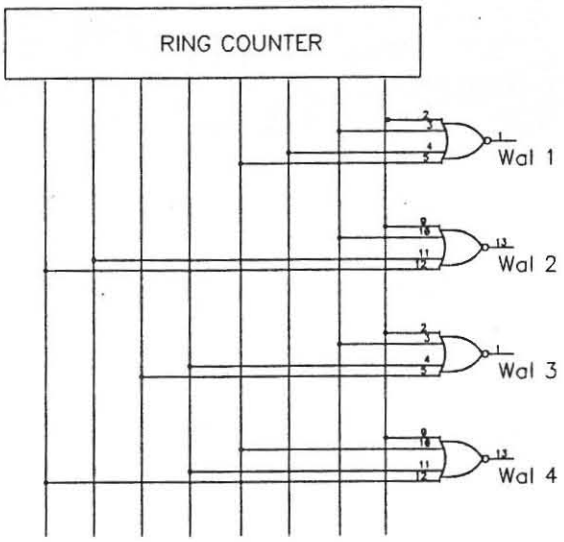

Fig.2.Walsh function generator.

In this circuit a clock pulse generator drives a ring counter which circulates a logic "1" through the counter stages.

The required outputs of the ring counter were combined in "NOR" logic gates to produce the set of Walsh functions. A number of different Walsh function generators are discussed by Beauchamp (1984:137), but the above method of added pulse generation was found to be particularly versatile for experimental purposes as the logic combinations may easily be altered if necessary.

3. MULTI-LEVEL SEQUENCY DIVISION MULTIPLEXING:

Although analog signals encountered in speech telephony may be multiplexed with a set of Walsh functions (Schreiber,1974: 323), only binary input signals have been used in the system which was constructed.

One of the important advantages of using the Walsh functions as carriers is that multiplication by digital data signals (modulation) produces only one sideband, and not two as is the case with sinusoidal products. (Beauchamp, 1987:185)

The reason is that the Walsh functions form a group under multiplication so that the product of two Walsh functions produces another Walsh Function.

$$Wal(n,t).Wal(m,t) = Wal(n \oplus m,t)$$

Where $\oplus$ is taken to mean modulo 2 addition of the indices n and m in binary form.

The production of a single sideband allows sideband filters to be omitted in SDM equipment.

A further advantage is that the circuitry consists largely of digital integrated circuits

also a multi-level waveform. A typical case is illustrated in fig. 5.

The upper trace is the original binary signal, and serves as a timebase or reference for the other signals in this figure. The second trace is the multilevel output signal from the corresponding demodulator.

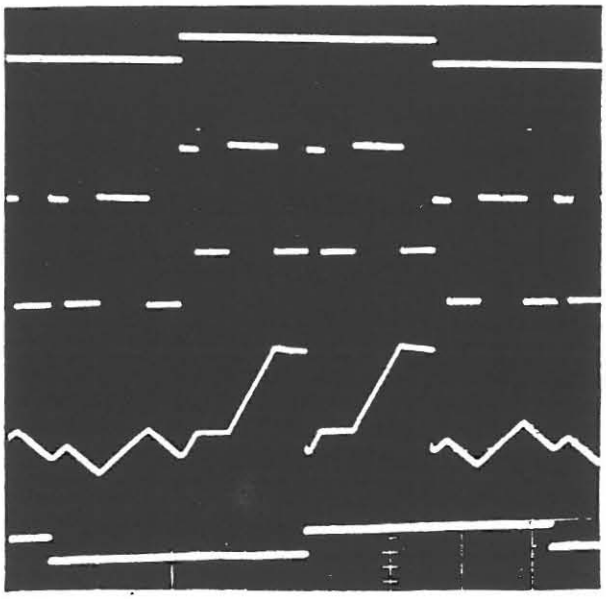

Fig.5. Demultiplexer waveforms.

3.3 Data recovery filter:

The multi-level output waveform from each demodulator is applied to an integrating circuit, and the output from each integrator is passed through a Schmitt trigger to a D flip-flop to recover the original data.

The process is illustrated by the third and fourth traces in fig. 5.

A successful system of this type has been installed in Switzerland, by Furrer, Shar and Maurer (1972:89).

This system is used to monitor a number of parameters from 50 measuring points along the length of an electric power cable installation.

4. BINARY DIGITAL SEQUENCY DIVISION MULTIPLEXING:

Multi-level signals have a variable peak to average power relationship and may be corrupted by noise. Such systems also require the use of very linear multipliers. (Beauchamp, 1984:238).

Titsworth (1963:42) proposed a system in which the multiplexed transmitted signal is also a binary signal with only two levels.

Gordon and Barrett, 1971 : 417 constructed an experimental system in which each codeword is scanned, timeslot by timeslot, and that character which is in the majority in each timeslot is taken as the signal to be transmitted.

The experimental system constructed at Technikon OFS is somewhat different in that the outputs from the modulators are first applied to a summing circuit, and then sliced at a level determined by the data inputs at the multiplexer.

A simplified block diagram of this system is given in fig. 6.

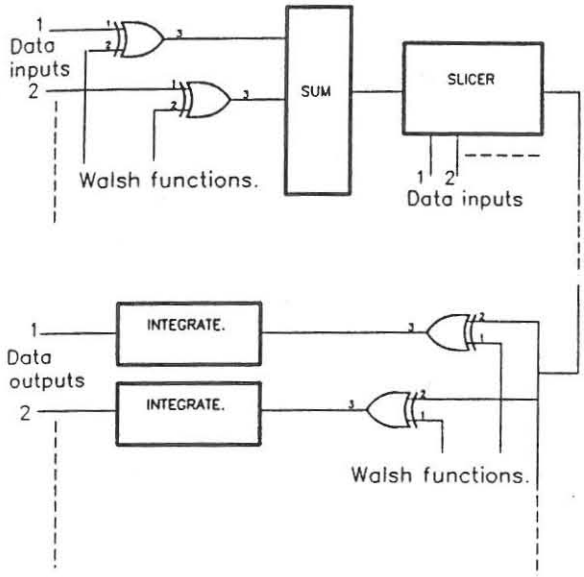

Fig.6. Binary sequency division multiplexing.

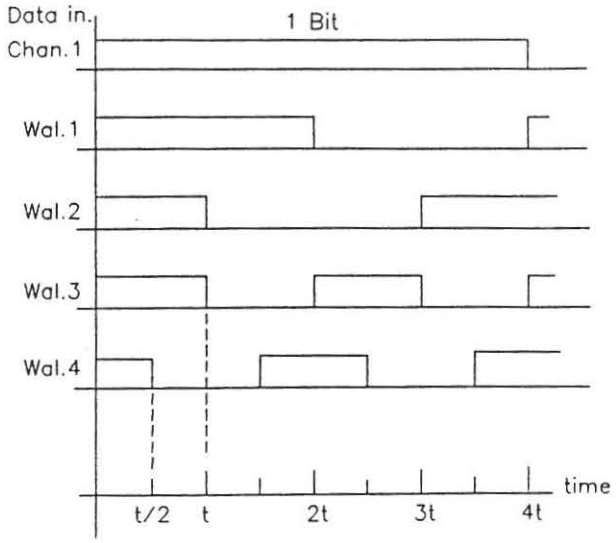

Fig.7 Timing of data and Walsh functions.

4.1 Modulation:

Simple exclusive "OR" logic was used to perform the function of modulation and demodulation.

For this reason, the Walsh functions which were used switch between 0 and 1, and not +1 and -1 as in the multi-level system.

Input data must be synchronous with the Walsh functions as shown in fig. 7.

The Walsh functions Wal3 and Wal4 determine the width of each timeslot t as in fig. 7 . For reliable signalling it was found by experiment that the duration of each data bit should not be less than four such timeslots.

A consideration of the Waveforms encountered during modulation and summation reveals that the multi-level signal extends over eight time periods, each of duration $t/2$.

This is due to the non-overlap in time of the functions Wal3 and Wal4 as shown in figs.7 and 8.

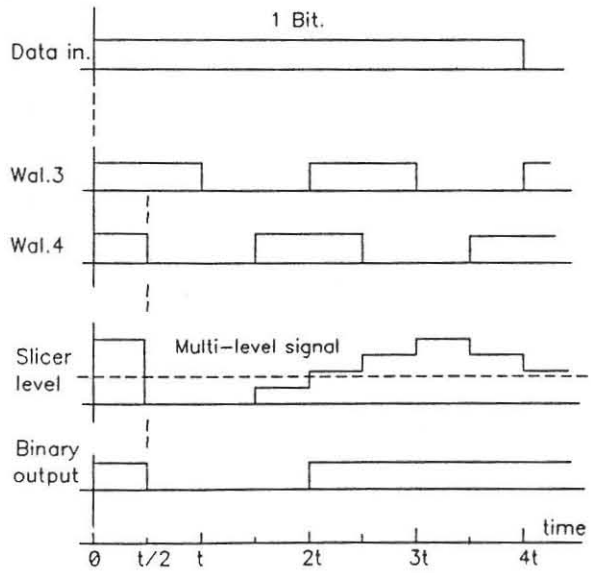

Fig.8. Slicer action.

4.2 Slicer:

The multi-level signal in fig. 8 is sliced at the second level and converted to a binary output signal with the aid of a comparator.

The slicing level required for each combination of data inputs was determined by inspection and proved experimentally.

Table 1 shows the slicing levels used for various data inputs.

Table 1

Data in.	Slicer.	Data in.	Slicer.
0 0 0 0	1	1 0 0 0	2
0 0 0 1	1	1 0 0 1	4
0 0 1 0	2	1 0 1 0	3
0 0 1 1	2	1 0 1 1	3
0 1 0 0	2	1 1 0 0	3
0 1 0 1	2	1 1 0 1	3
0 1 1 0	3	1 1 1 0	4
0 1 1 1	3	1 1 1 1	4

A programmable array logic (PAL) circuit was used to set the correct level for each combination of data inputs.
Binary output signals for each data bit extend over eight periods of $t/2$ and may be transmitted in the form shown in fig. 8.

4.3 DEMODULATOR:

The binary signal is demodulated by the corresponding Walsh functions at the receiver. Exclusive "OR" circuits were used for this purpose.

The output from each demodulator is also a binary signal that extends over eight periods of $t/2$ for each data bit. Waveforms of demodulation process are illustrated in fig. 9.

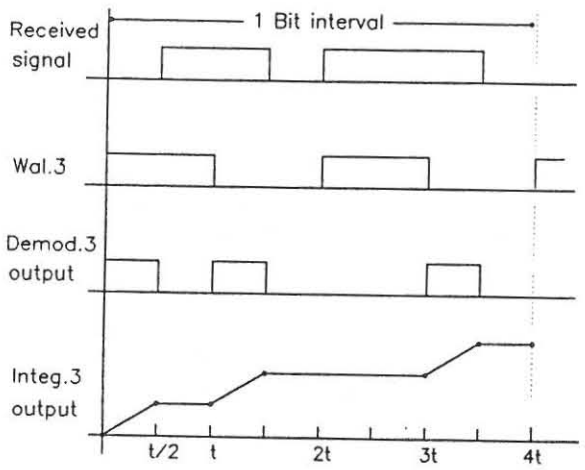

Fig.9.

Demodulation of received binary signals.

The number of 1's in each interval of 8 x $t/2$ determines whether a data 0 or 1 has been received.

In the system constructed, three or less 1's represents a 0 bit, while five or more 1' represents a 1 bit.

An integrating circuit followed by a Schmitt trigger and D latch is used to recover digital data from the demodulator outputs as shown in fig. 9.

The complete multiplexing/de-multiplexing process for several data combinations is shown by the waveforms in fig. 10. (see addendum A)

5. SYSTEM EVALUATION:

A novel pseudo random data generator has been constructed to facilitate testing of the equipment. A test set which allows data input signals to the multiplexer to be compared with output signals from the demultiplexer has been built to permit detection and counting of errors.

Performance tests of the systems are presently being conducted.

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Addendum A.

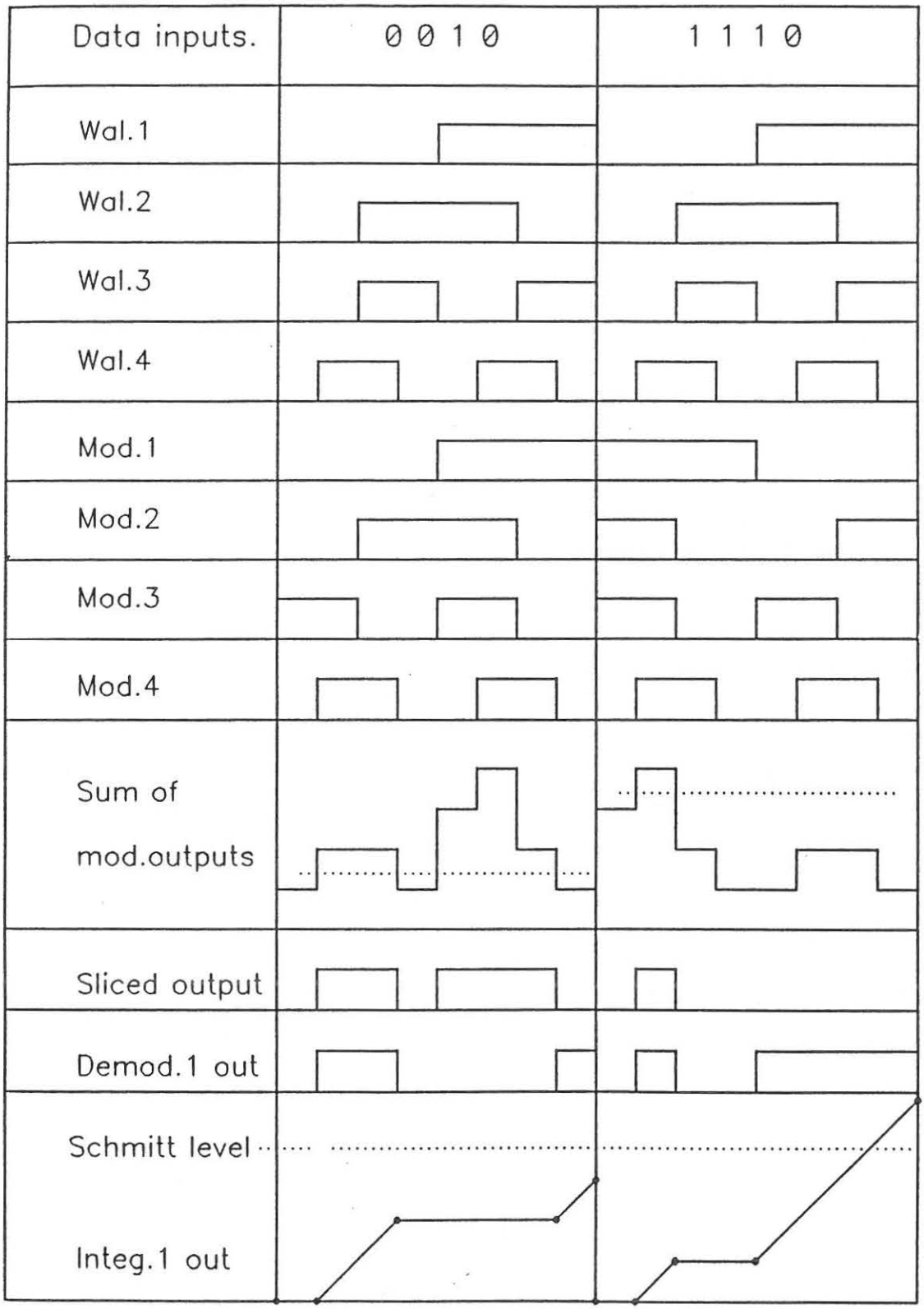

Fig.10. Binary sequency division multiplexing waveforms.

APPENDIX G

IMPLEMENTATION OF AN ADAPTIVE SLICER IN A BINARY WALSH CODE TRANSMISSION SYSTEM

POSTER

PRESENTED AT THE 13TH INTERNATIONAL CONFERENCE

UNIVERSITY OF APPLIED SCIENCES

MITTWEIDA, GERMANY

NOVEMBER 1998

IMPLEMENTATION OF AN ADA[illegible]N A BINARY WALSH CODE DATA TRANSMISSION SYSTEM

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Technikon Free State - Bloemfontein - South Africa

Abstract: The transmission of digital information in a binary multi-channel system using Walsh functions as carriers requires a means of converting multi-level signals to binary signals that will readily permit the recovery of data. An adaptive slicer that is set by the combination of signals at the inputs to each channel was developed for this purpose.

Fur die Übertragung von digitalen Informationen in einem binären Mehrkanal-System, wobei Walsh-Funktionen als Träger benutzt werden, wird eine Technik benötigt, durch welche man Multi-level Signale umwandeln kann. Dies lässt die Wiederherstellung der Daten zu. Fur diesen Zweck wurde eine Kombination von Komparatoren ("Slicer") entwickelt. Der Slicer wird über seine Eingänge progammiert.

Introduction

The work in this project was concerned mainly with the use of a set of orthogonal square waveforms as carriers in a multi-channel system for the transmission of digital information for telemetry applications. The set of square waveforms used as carriers are known as "Walsh functions" [1].

The Walsh functions are a set of aperiodic rectangular waveforms and since the number of zero crossings per second is irregular the term "sequency" is used in place of "frequency" [2].

Sequency division multiplexing is similar to frequency division multiplexing in that the input signals also modulate carriers that are allocated to each channel. In other ways, as the Walsh functions are pulses, sequency division multiplexing resembles time division multiplexing [3]. A four channel sequency division multiplexing system was constructed using a set of four Walsh functions as carriers.

In this application the input signals to each channel consisted of data pulses in binary form. Each input signal modulates one particular Walsh carrier from the set of Walsh functions. The modulator outputs are combined in a summation process producing a multi-level signal which must be converted to a binary signal before transmission [4].

By inspection of the waveforms it can be seen that if the output of the summing network is sliced at a fixed level the signals cannot be decoded correctly for all input data combinations. However, by setting the slicing level according to the combination of the input data during each bit interval the original signals can be recovered at the receiver.

At the receiver, the demodulator recovers the data in each channel by multiplying the composite waveform with locally generated replicas of the Walsh function carriers. The output of each demodulator consists of a series of pulses and these are applied to integrator circuits which are reset at the end of each data bit.

2. Binary sequency division multi[illegible]

A simplified block diagram of the binary sequency multiplexing system is given in Fig. 1.

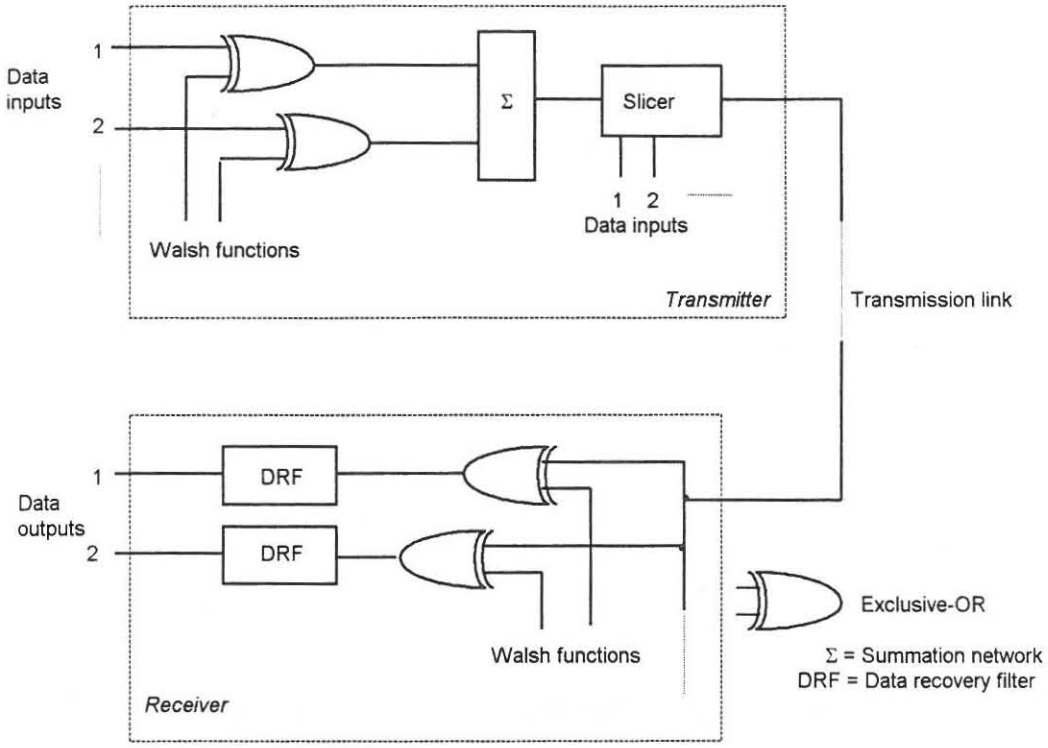

Fig. 1 *Block diagram of binary sequency division multiplexing system*

Exclusive-OR logic was used to perform the function of modulation and demodulation. The *exclusive*-OR modulator outputs are combined in a linear summing network and the composite multi-level signal is applied to the slicer. The action of the transmitter is illustrated by the waveforms in Fig. 2.

The output from each demodulator is a binary signal consisting of a number of pulses within each bit period. At the receiver the binary signals are demodulated by the corresponding Walsh functions in *exclusive*-OR logic circuits.

The output of each demodulator is applied to a data recovery filter containing integrators, Schmitt triggers, and D flip-flops to recover the data bits. The number of 1's in each interval of eight *t*/2 periods determines whether a data 1 or 0 has been received. The Schmitt trigger uses the integrator output at the end of the integrating period to establish whether a 1 or 0 condition exists. Note that there is an inherent 1 bit delay between the input and output pulses to the system.

The process of demodulation is illustrated by the waveforms in Fig. 3.

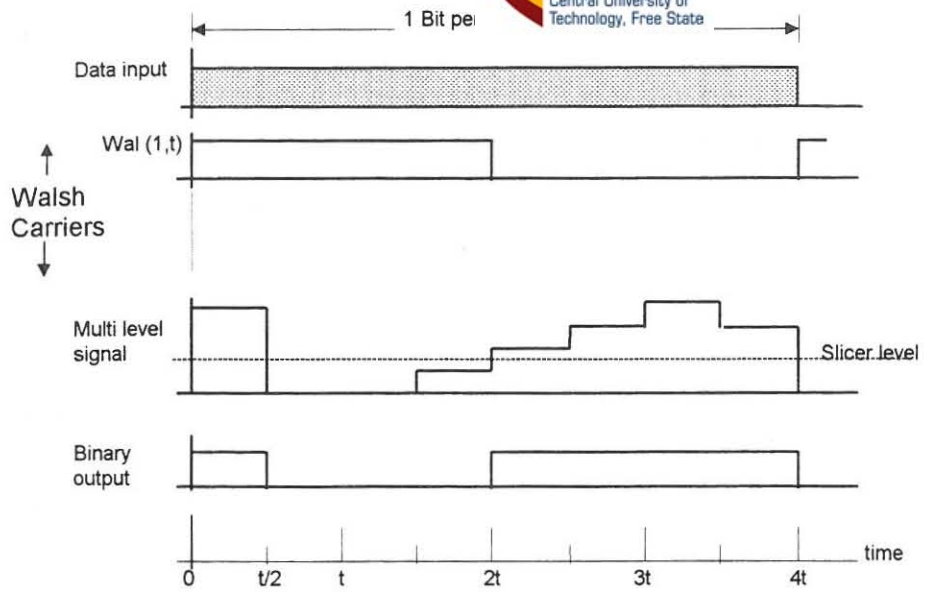

Fig. 2 *Sequency multiplexing transmitter action.*

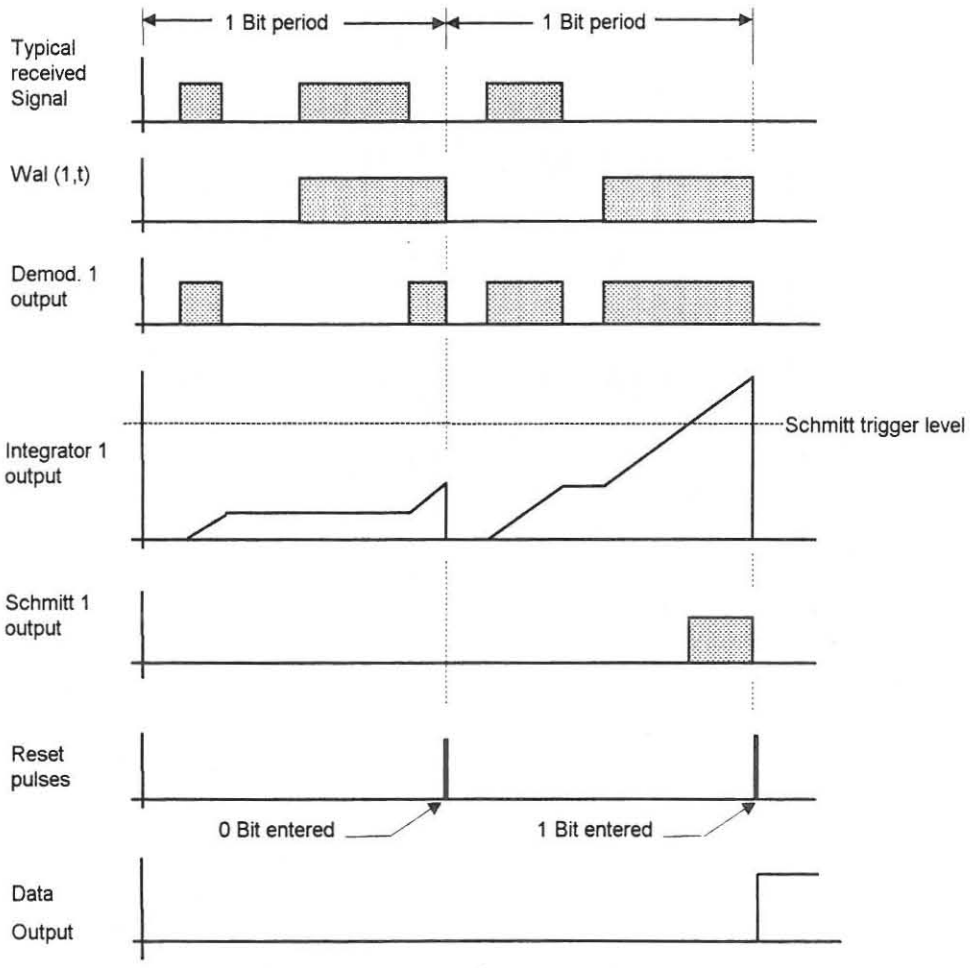

Fig. 3 *Demodulation of typical binary sequency multiplexing signal*

3. Adaptive slicer

By sketching the relevant waveforms for each combination of data inputs it can be seen that if the output of the summing network is sliced at a fixed level the signal cannot be decoded correctly for all input data combinations. However, by setting the slicing level according to the combination of data inputs during each bit interval the original signals can be recovered at the receiver.

The slicing level required for each combination of data inputs can be determined by inspection and proved experimentally. The optimum slicing levels found for reliable demultiplexing of various data inputs are given in table 1.

Table 1 *Slicing levels for all data input combinations*

a	b	c	d	Slice level
0	0	0	0	w
0	0	0	1	w
0	0	1	0	x
0	0	1	1	x
0	1	0	0	x
0	1	0	1	x
0	1	1	0	y
0	1	1	1	y
1	0	0	0	x
1	0	0	1	z
1	0	1	0	y
1	0	1	1	y
1	1	0	0	y
1	1	0	1	y
1	1	1	0	z
1	1	1	1	z

Since the combinational logic required to perform the slicing function requires a large number of gates, a 16R4 programmable array logic (PAL) integrated circuit has been used for this purpose. [4]].

A set of Boolean relations can be derived from this table and used to prepare a programmable array logic (PAL) circuit to accomplish the logic required for the slicing circuit.

The outputs of the PAL must be con way that the slicer is set more or less in the centre of each amplitude level for the various combinations of data inputs.

Output W must set the slicer to the lowest level, output X sets it to the next higher level, output y sets it to third level and output Z sets it to the highest level. The different levels are obtained by weighting the outputs of the PAL in a summing network.

The PAL is connected to the weighted summing network as shown in Fig.4.

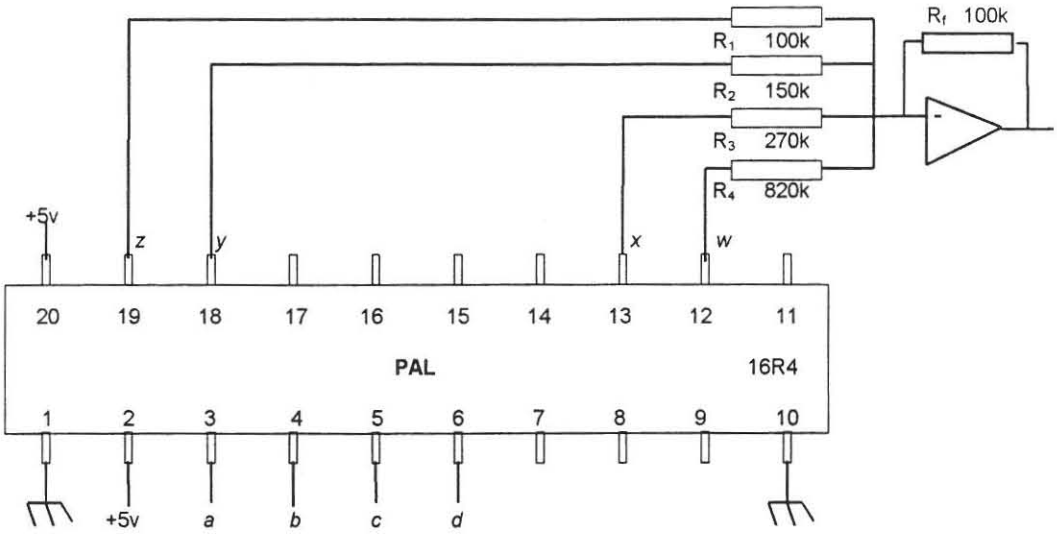

Fig. 4 *Connection of PAL in circuit*

4. Comparator

During the time interval of each data bit the outputs of the modulation summing circuit is compared with the level set by the PAL logic circuit. The comparator circuit with the linear and weighted summing amplifiers is given in Fig.5.

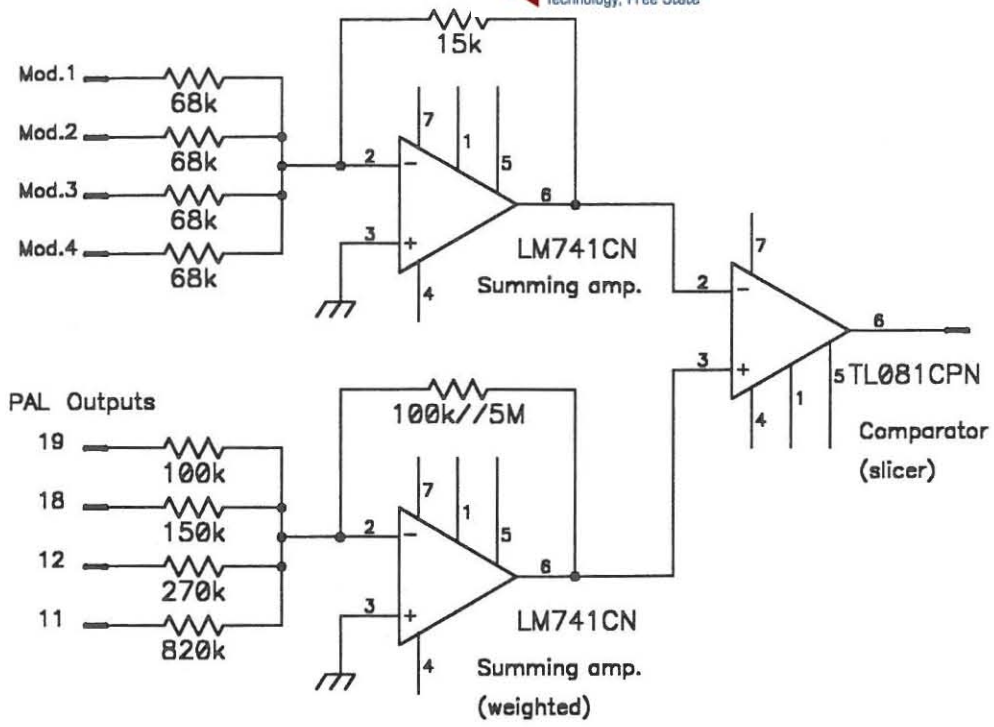

Fig. 5 *Comparator Slicer*

A TL081 operational amplifier was used in a standard comparator circuit.

5. Conclusions

The system performance was evaluated using a random data generator for the data inputs and white noise was added to the transmitter output to determine the bit error rate. The results have indicated that provided the channel bandwidth is adequate the system operates satisfactorily for use in telemetry applications.

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